



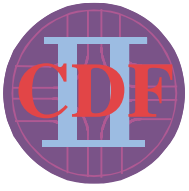
The Run IIB Silicon Upgrade

Outline

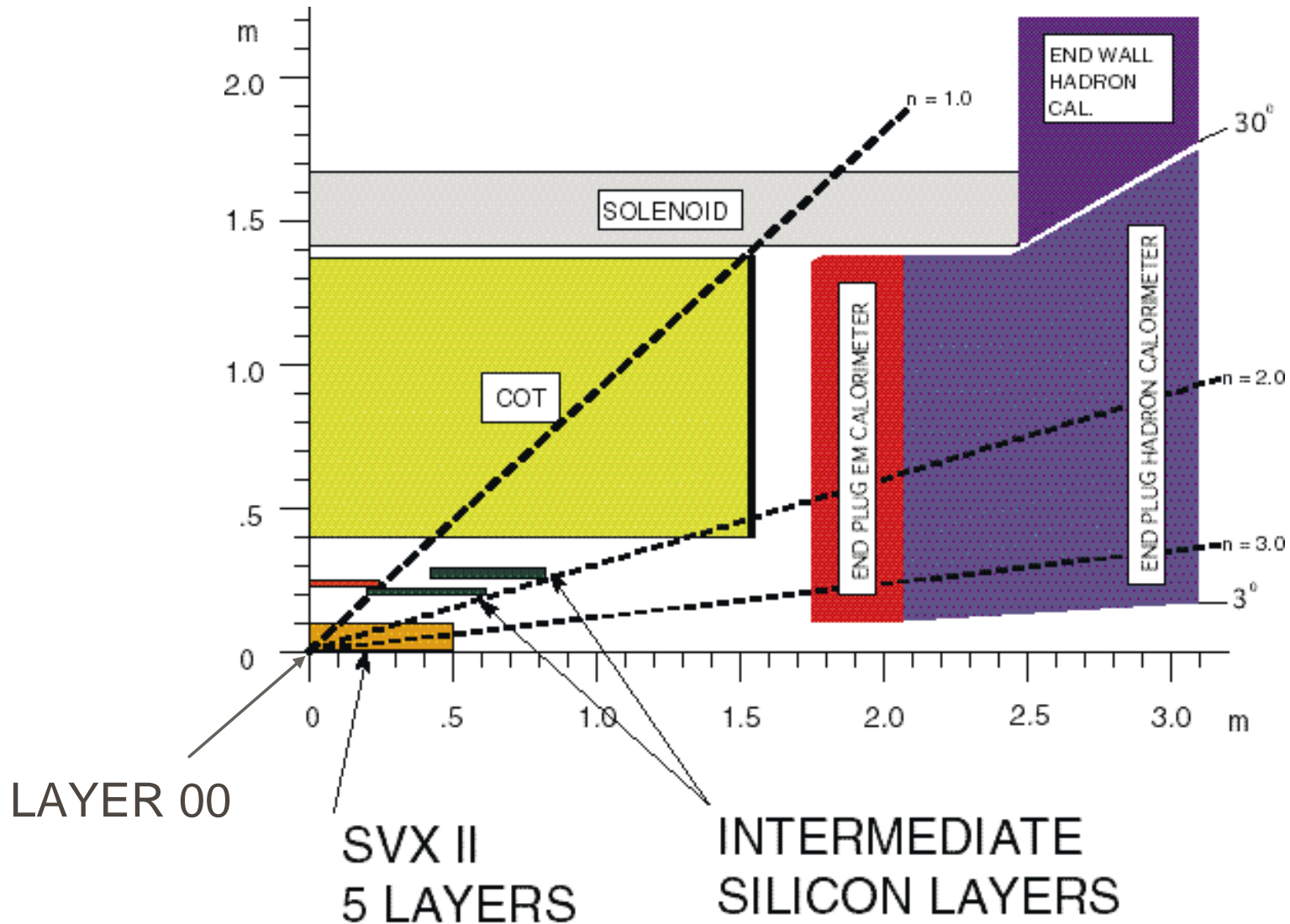
- ❑ Run IIA silicon: *what's there and how it got there*
- ❑ High luminosity Run IIB: *Higgs sought*
- ❑ Some problems, some solutions: *the upgrade*
- ❑ UCD plans

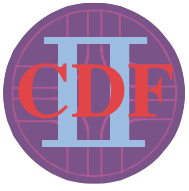
Physics 295 (*not a free lunch...*)

Feb. 20, 2002

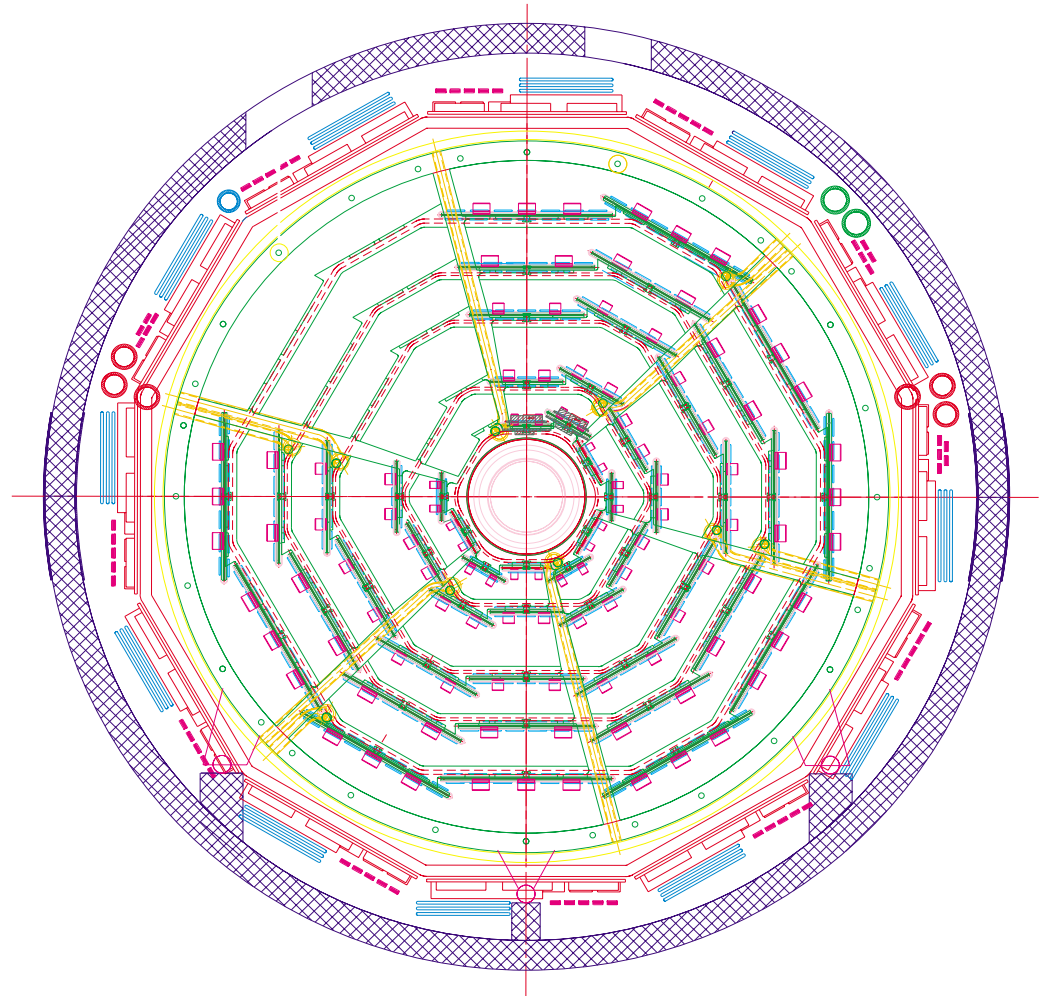
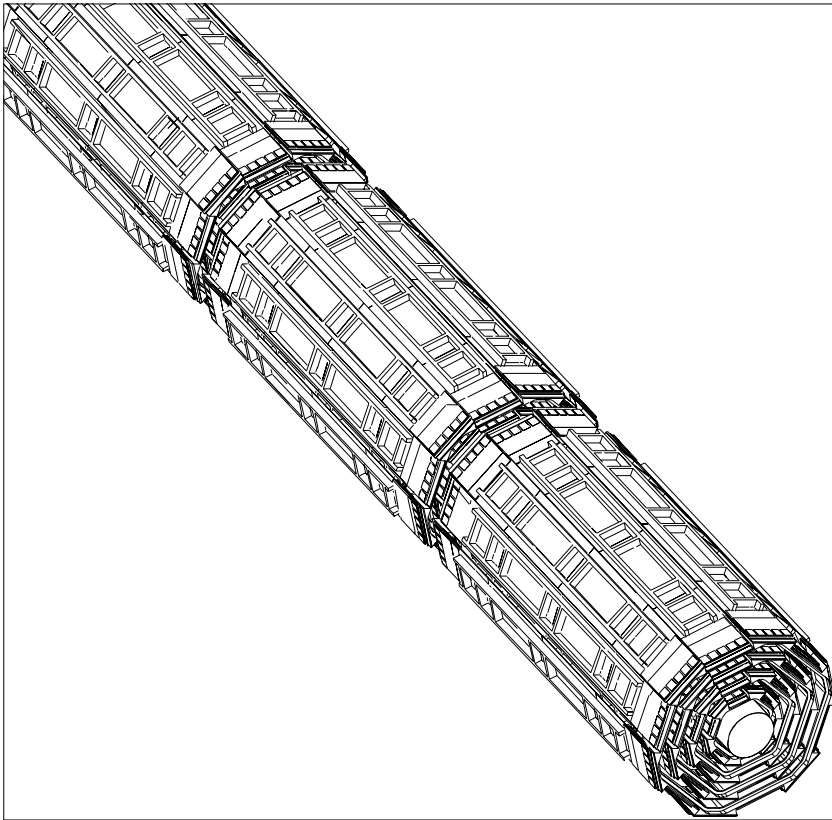


Quadrant of CDF II Tracker



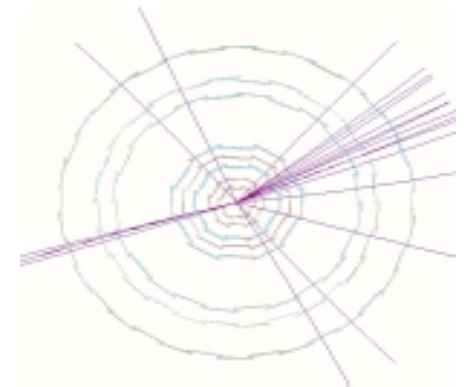
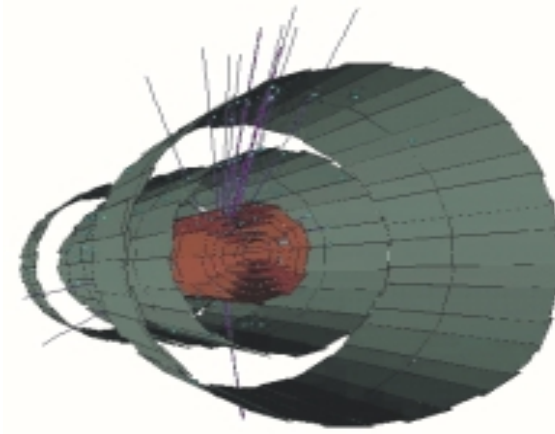
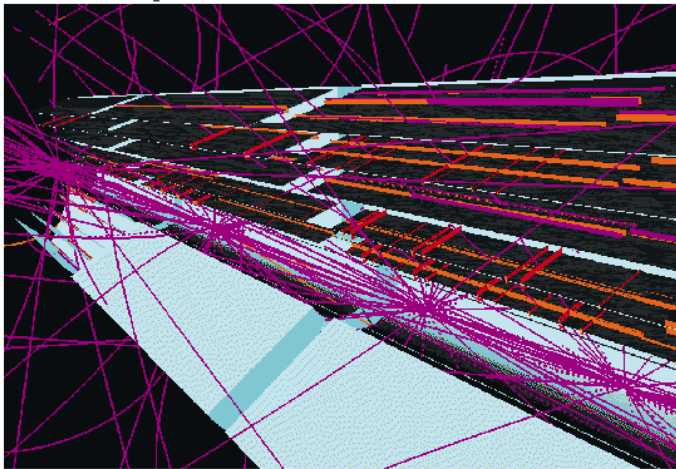
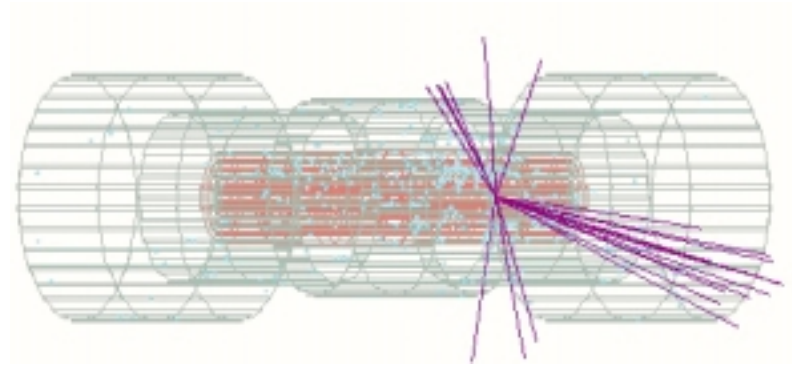
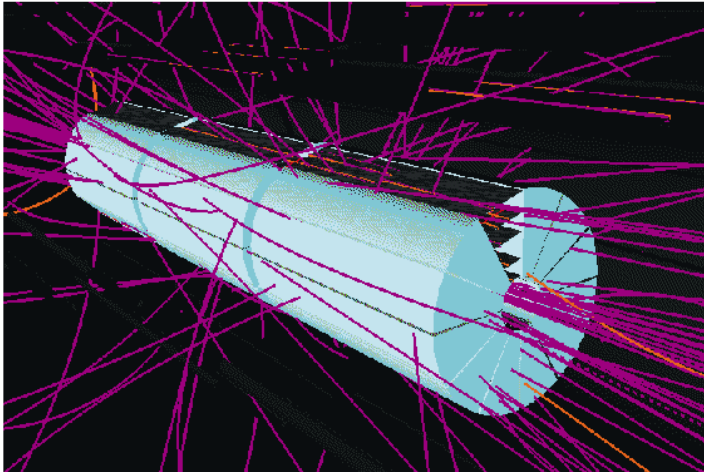


SVX II: 3 Barrels, 5 Layers





Simulation: Run II CDF Si



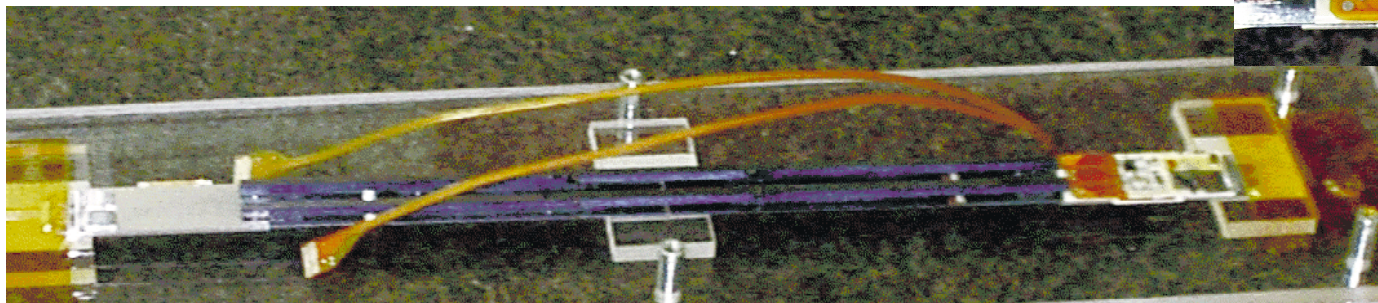
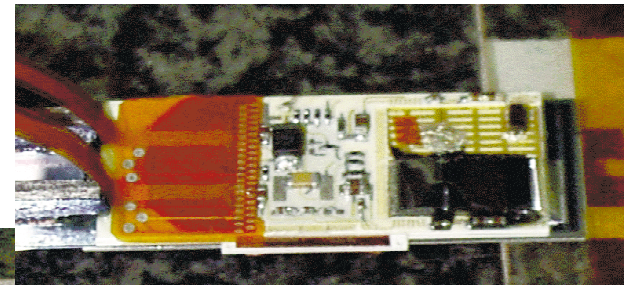
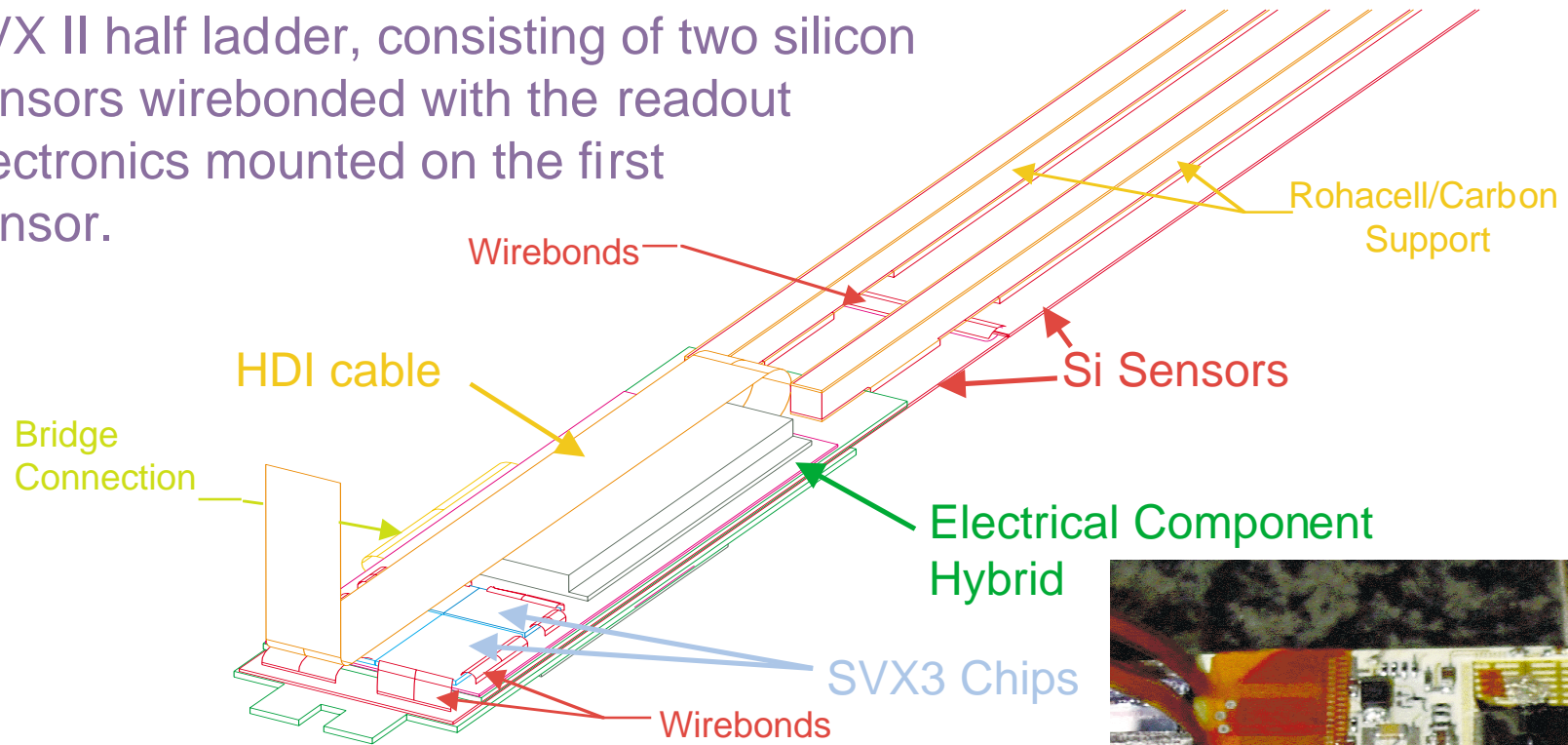
Open Inventor based

ROOT based



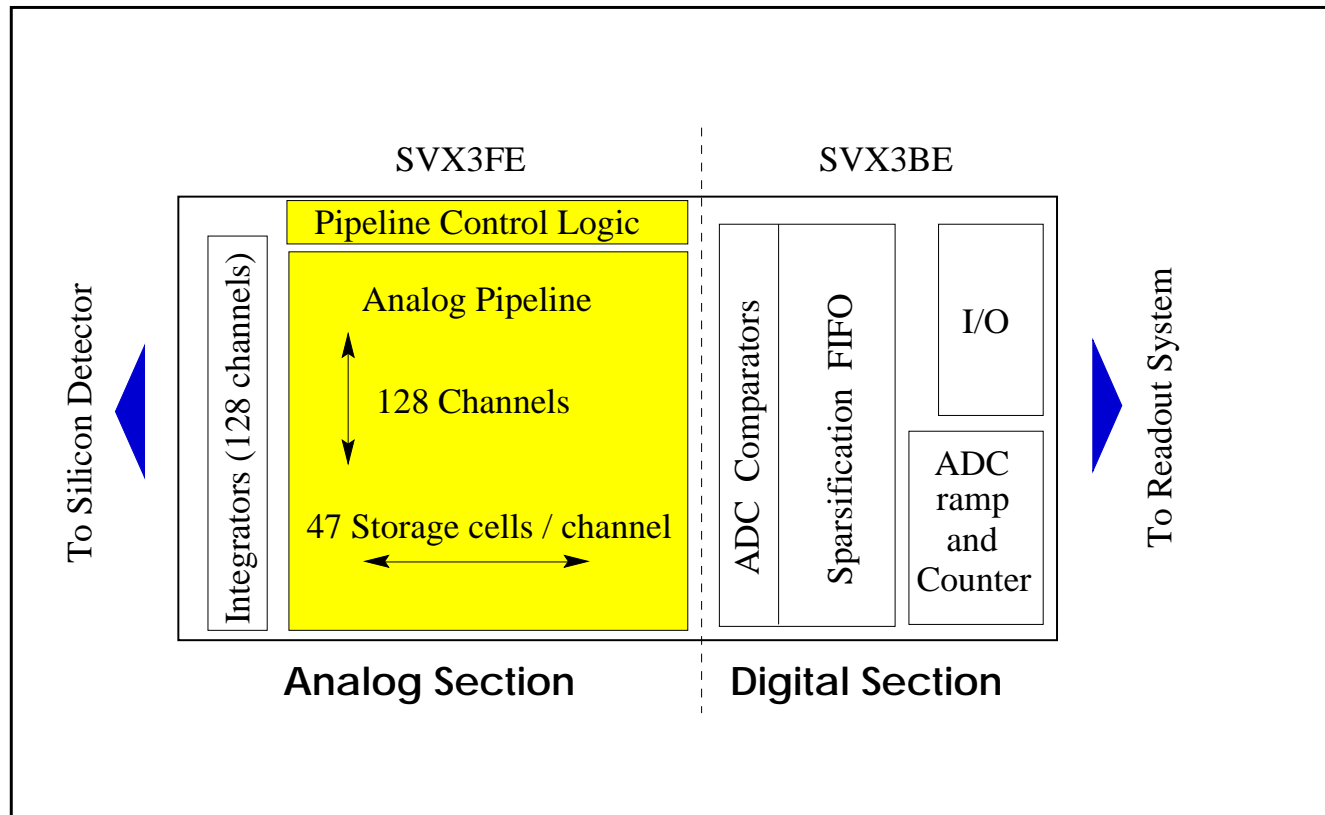
SVX II Ladders

SVX II half ladder, consisting of two silicon sensors wirebonded with the readout electronics mounted on the first sensor.

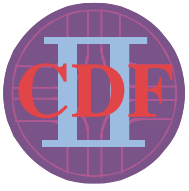




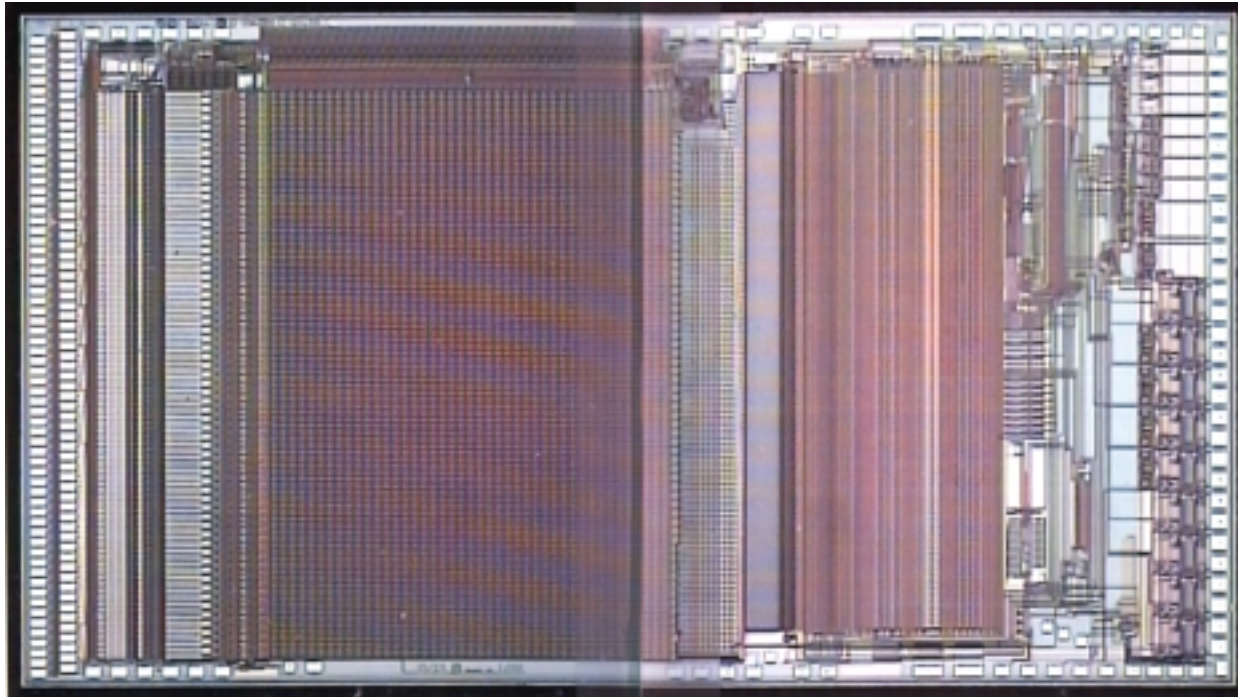
SVX3D R/O Chip



- Rad-hard 0.8 um Honeywell CMOS
- Tested to ~ 4 MRad
- Deadtimeless
- Dynamic pedestal subtraction
- Common to all Run II CDF silicon projects



SVX3D R/O Chip





UCD Students on Run IIA Silicon

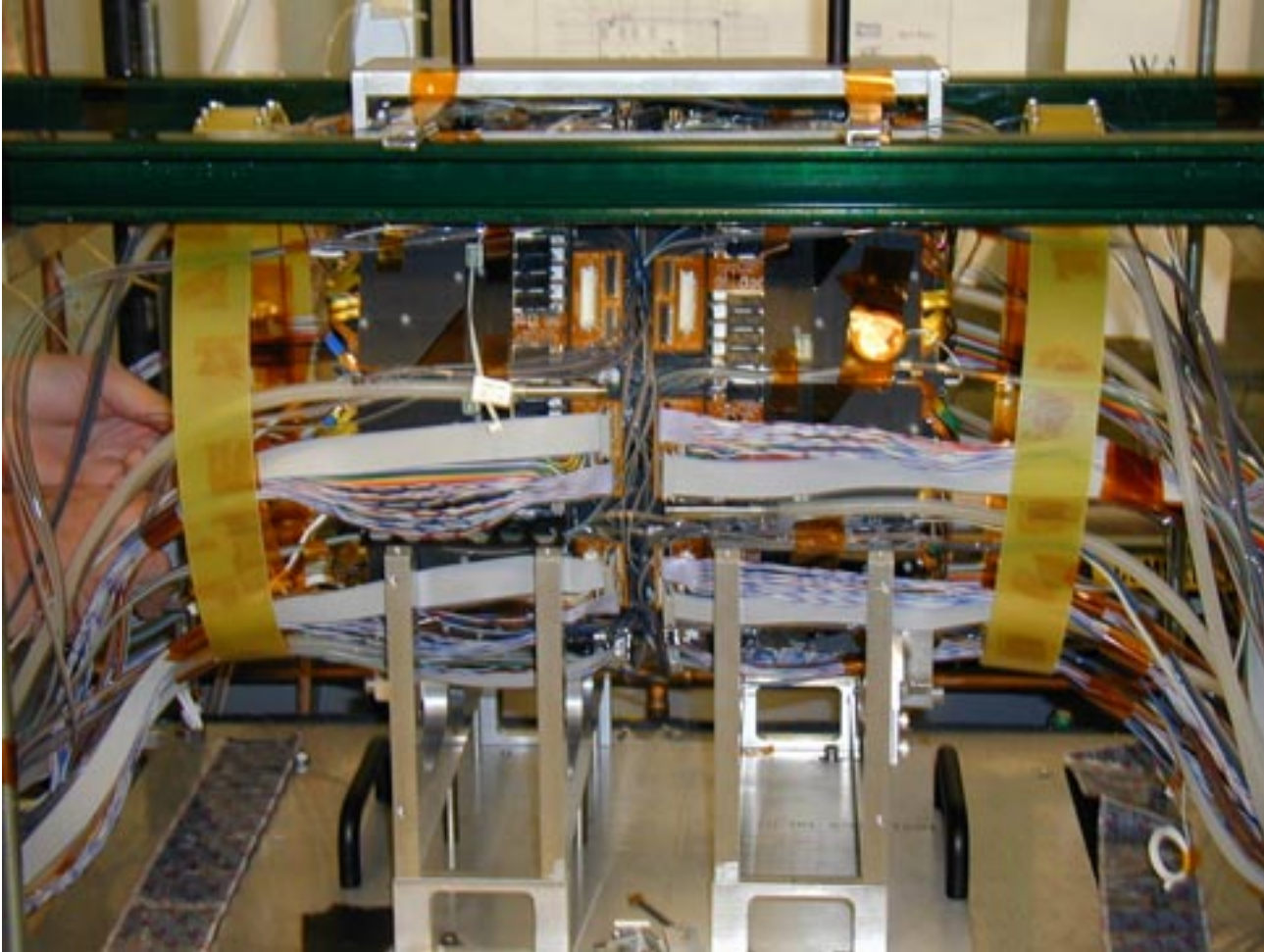
- UCD students on Run IIA silicon (ISL and Layer 00):
 - Sasha Barioant
 - Paul Gomez (UG, post-graduate researcher)
 - Chris Hill (graduated, now at UCSB, co-leader of CDF Silicon)
 - Tiffany Wilkes

*Right:
Chris Hill at work
on his thesis*



Last Collab Meeting...

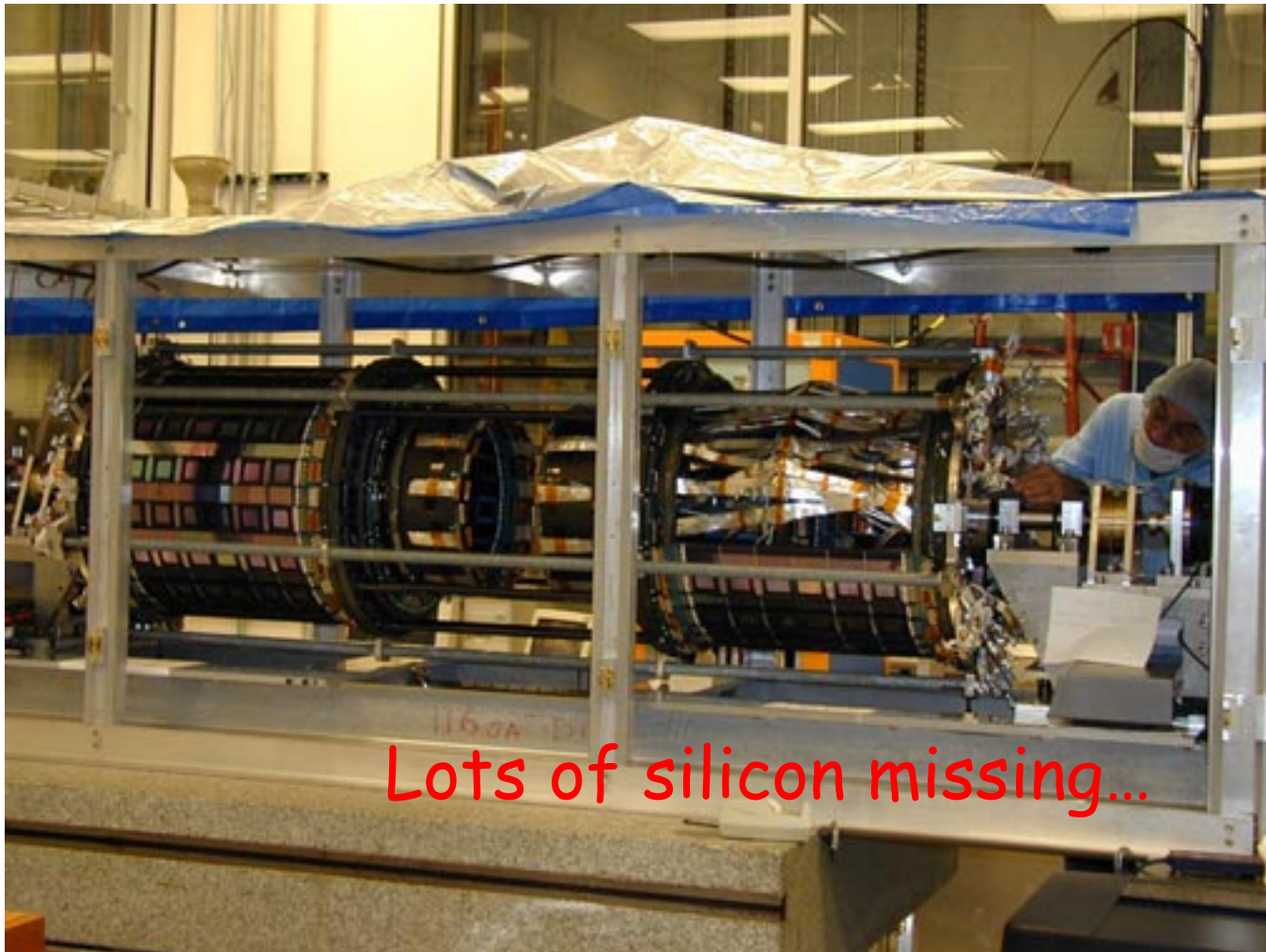
- SVX looked like this:



2 barrels in
spacetube
and
working to
finish
Barrel-3

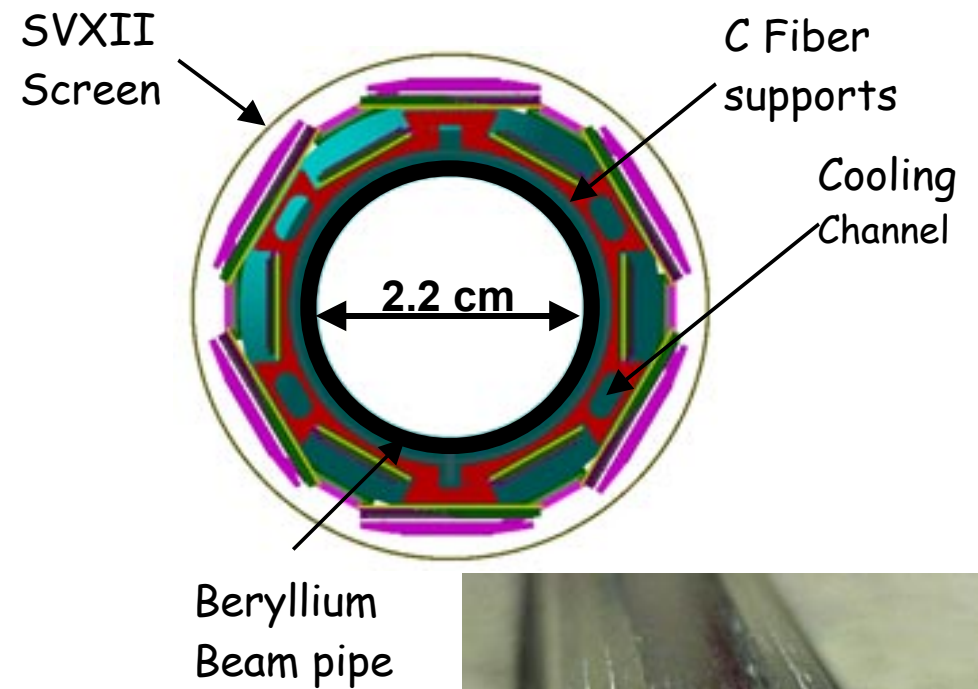
Last Collab Meeting...

- ISL looked like this:



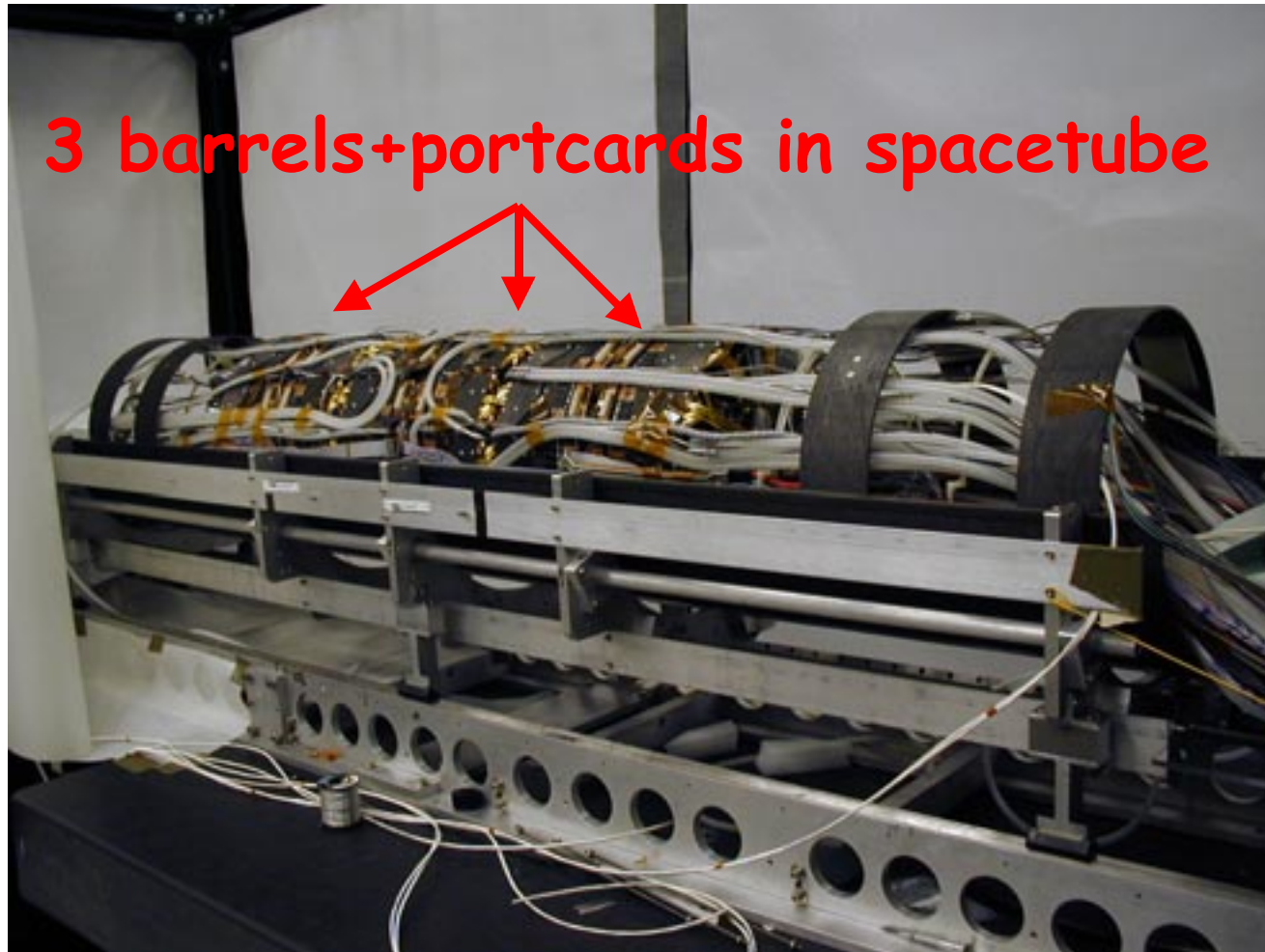
Last Collab Meeting...

- Layer 00 was still a cartoon...



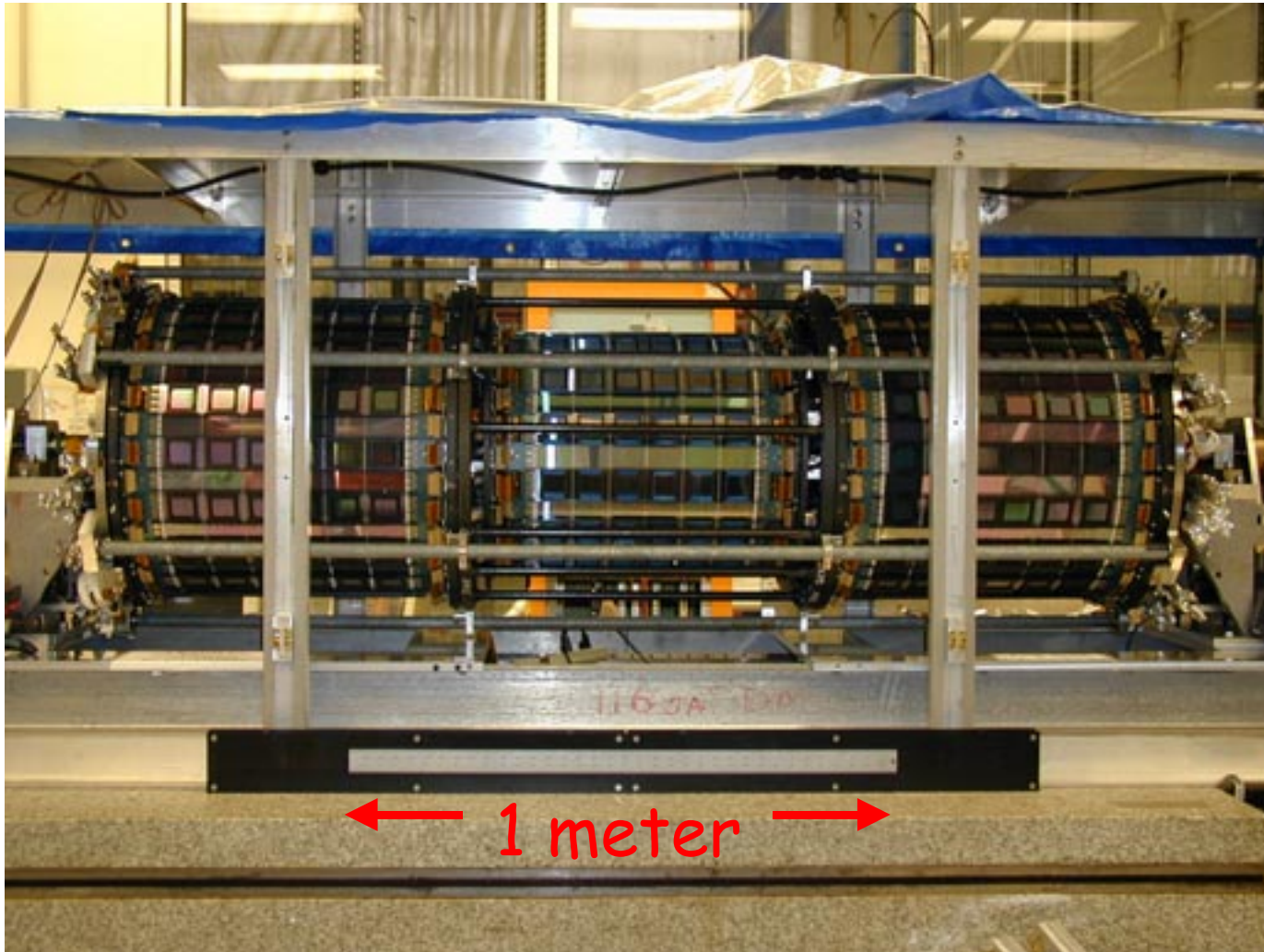
About 2 wks later...

- SVX looked like this:



About 2 wks later...

- ISL looked like this:



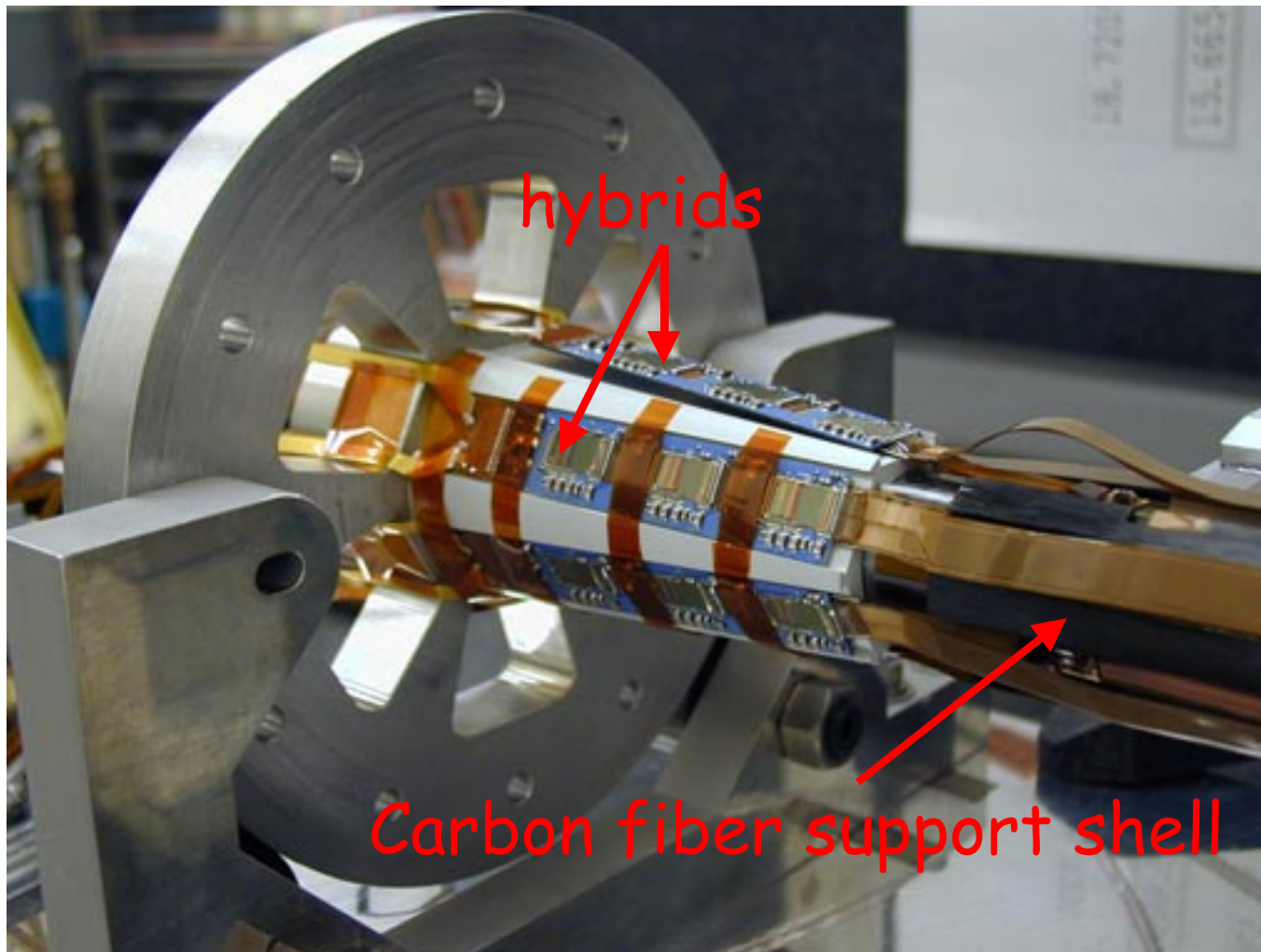
25-Jan-01

D.Glenzinski, Collaboration Meeting

6

By November...

- L00 looked like this:



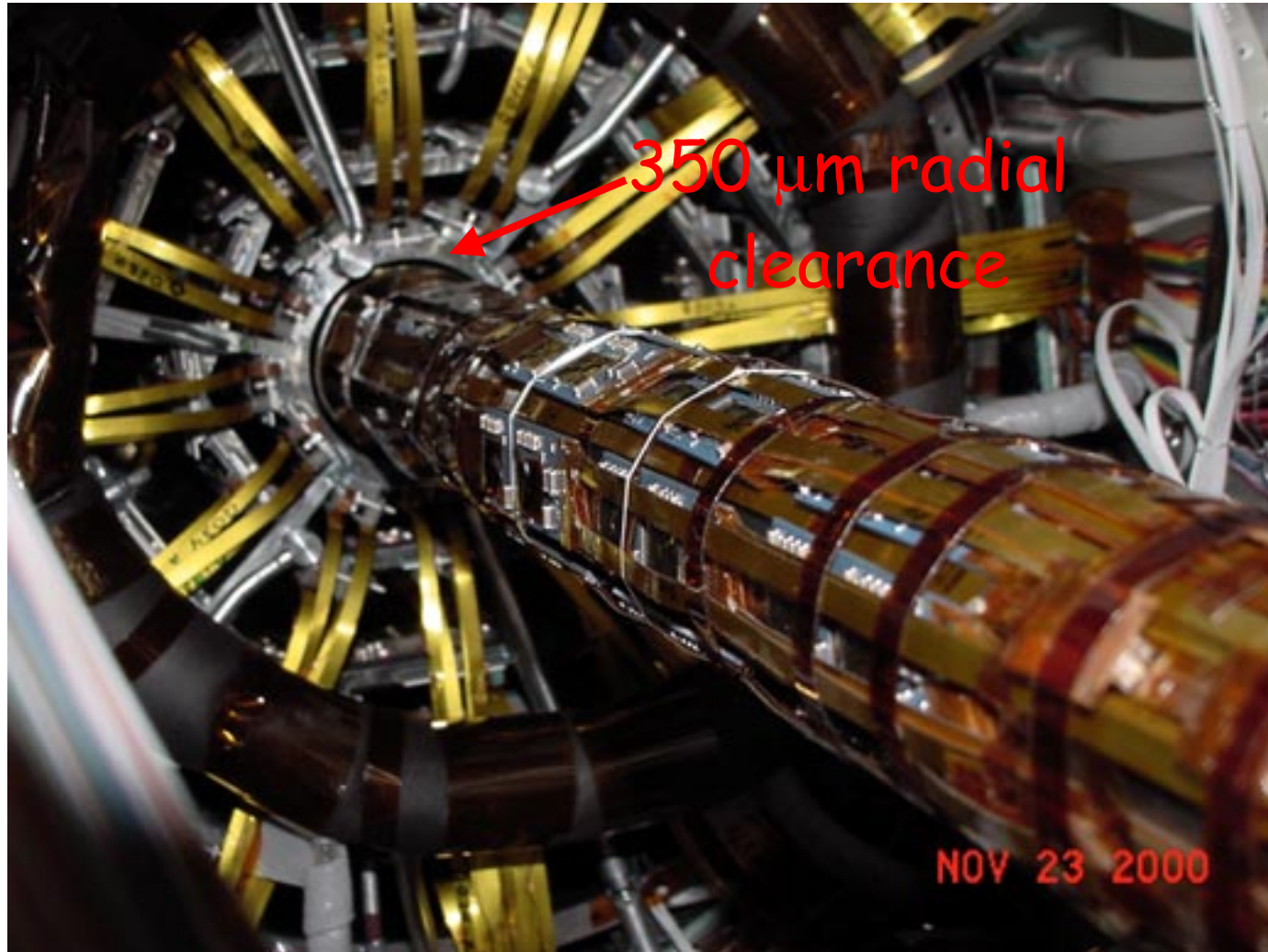
25-Jan-01

D.Glenzinski, Collaboration Meeting

7

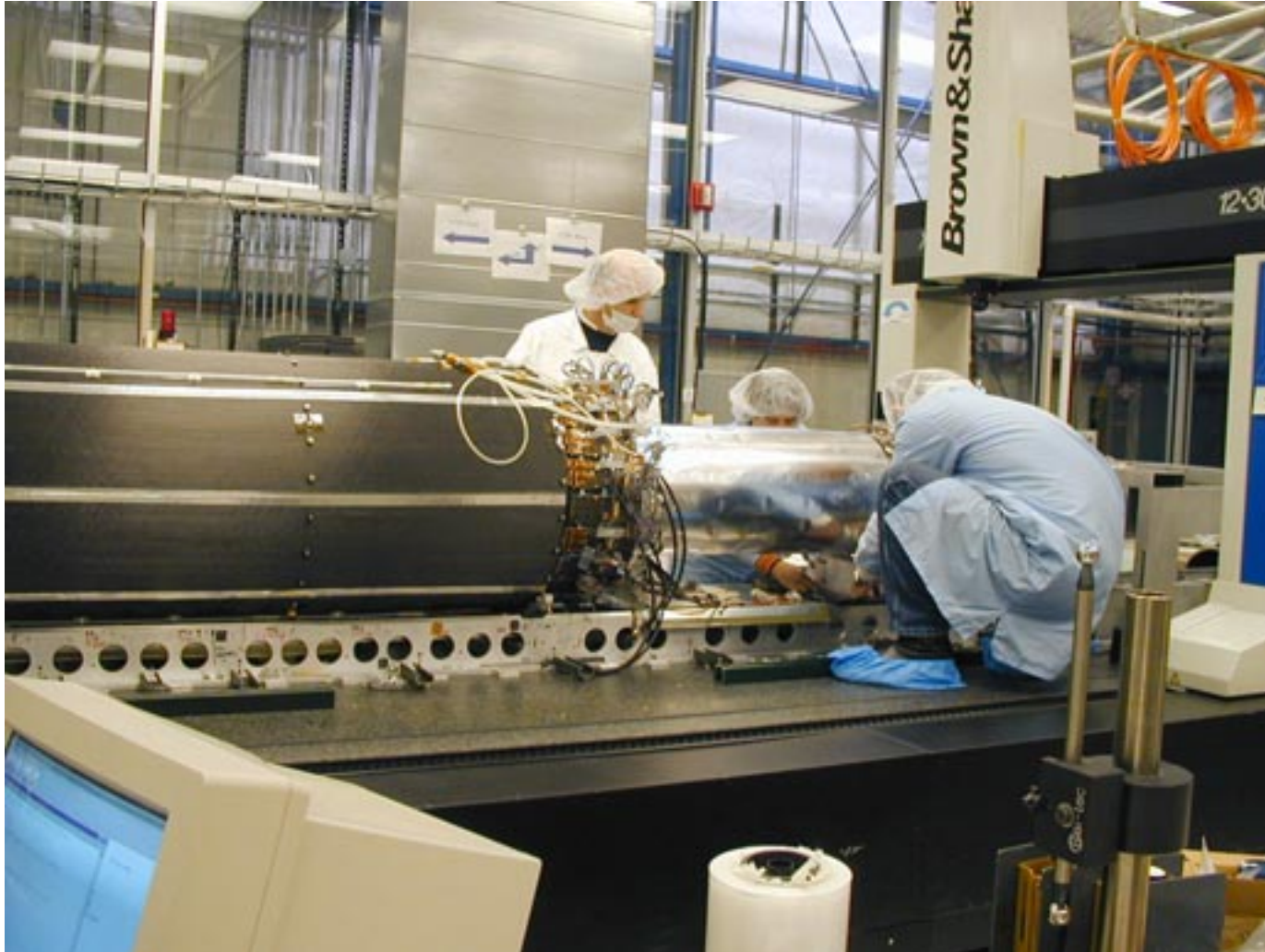
By end November...

- L00 installed inside SVX:



By end December...

- SVX/L00 installed inside ISL:



25-Jan-01

D.Glenzinski, Collaboration Meeting

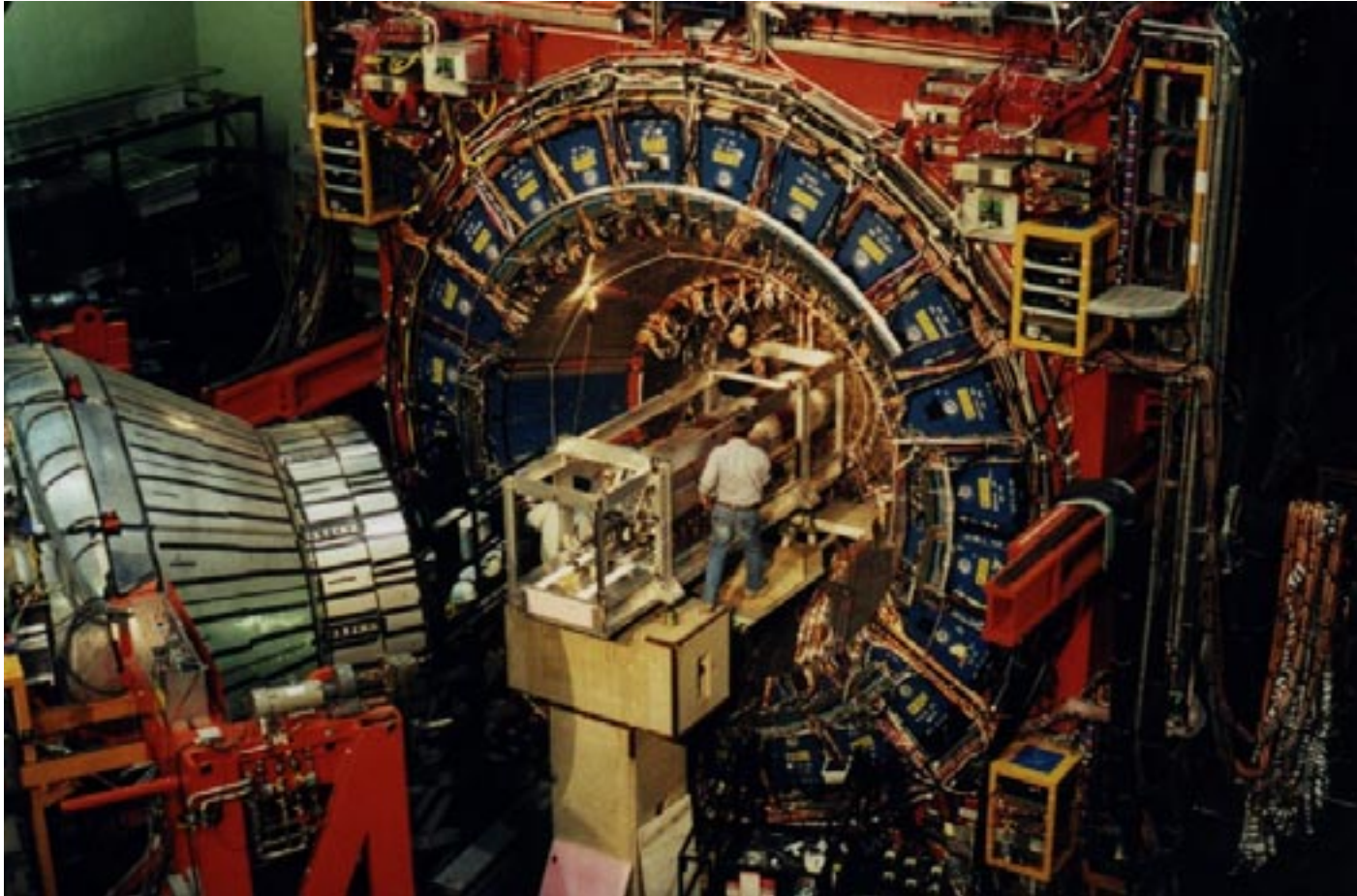
9

16-January-01: The Move



everything went exactly
as planned -

16-January-01: The Installation



The CDF
Run2
Silicon
Detector
was
installed
inside the
COT at
around
2200 on
16-Jan-01

25-Jan-01

D.Glenzinski, Collaboration Meeting



Run 2b

- FNAL Supports extended running: $\sim 15 \text{ fb}^{-1}$ per experiment by 2007
- Laboratory proposed the following boundary conditions for the Run 2b upgrade projects.
 - The budget for the replacement of silicon vertex detectors should be 2.5M\$ per experiment, with contingency
 - The new detectors must be designed with the confidence that they will operate effectively throughout Run 2b, with an anticipated luminosity of at least 15 fb^{-1}
 - The installation of all detector upgrades must occur during a single shutdown of no more than six months duration, with roll-out and roll-in tentatively scheduled between October 2003 and March 2004.



Run 2b Working Group

- Run 2a silicon
 - Designed to survive 2 fb^{-1} with high degree of confidence.
 - The most appropriate rad-hard technology available at the time
- Run 2b Working Group: Address the following questions
 - Given the new luminosity goal how long will the silicon survive ?
 - If necessary: What are the simplest and most effective strategies for replacements ?
 - Incorporate all of our experience over the past decade
 - Use newer technologies to our benefit



Run 2b Silicon Study Group

16 Institutions (so far)

Carnegie Mellon, Davis, Duke, FNAL, Hiroshima, INFN-Padova, JINR-Pittsburgh, LBNL, New Mexico, Okayama, Pittsburgh, Purdue, Rutgers, Texas Tech, Toronto, Tsukuba



Working Group Achievements

- Identified lifetime of present system
 - The issue is depletion voltage and noise
 - Important caveat: There exist a limited number of direct measurements in actual Tevatron environment. These have some inconsistencies.
 - Ionizing component (surface damage at 3 cm)
 - Run 1a data \Rightarrow 300 rad/pb⁻¹
 - Run 1b data \Rightarrow 600 rad/pb⁻¹
 - Leakage currents (damage to nuclear lattice)
 - Run 1a data \Rightarrow 0.8 nA/strip/pb⁻¹
 - Run 1b data \Rightarrow 0.6 nA/strip/pb⁻¹
 - Average radial dependence R^{-a} where $a = 1.5$ to 1.7
 - Extrapolations to very small radii (L00) have large uncertainty
 - Beyond these measurements, we rely upon published radiation damage studies which do not mimic actual operating conditions \Rightarrow interpretations, uncertainties
 - Dose rate is much higher
 - Specific particle types and energies are used
 - What engineering safety margin is appropriate ?
 - LHC is using factors of 1.5 to 2.0



Lifetime calculations

- Run 2a detector design:
 - *guaranteed* to last 2 fb⁻¹, should last longer. But how long ?
- Evaluate two characteristics of each layer on the basis of known operation and available data on radiation damage:
 - Signal-to-Noise Ratio (SNR)
 - Bias voltage required for full depletion (V_D).
- Rad-damage mainly nuclear reactions in bulk
 - Leads to both higher leakage current (I_L) and change in dopant concentration which affects the depletion voltage
 - We can begin to understand I_L with relatively modest doses.
 - To determine V_D in CDF we need larger doses - i.e. Run 2a data.
 - Run 1 data: direct normalization of I_L vs integrated luminosity L.
$$I_L = 1.13 \text{ mA} \times V_s \times R^{-1.7} \times L^{-1} \quad V_s = \text{Strip Volume (units are cm and fb}^{-1}\text{)}$$



Longevity by layer

Layer	R_{\min} [cm]	Lifetime limits [fb^{-1}]		no p-side bias		Cause of Death
		" 1σ "	Central	" 1σ "	Central	
L00 (10%)	1.35/3	4.5	5.5			SNR
L00 (10%)	1.35/5	6.5	9.0			SNR
L00 (80%)	1.62/7	8.0	11.0			SNR & V_D
L0 ϕ or z	2.54	5.2	7.9			V_D
L1 ϕ -side	4.12	12.0	18			V_D
L1 z-side	4.12	12.0	17			V_D
L2	6.52	10	16	3.8	6.0	V_D
L3 ϕ -side	8.22	38??	76??			V_D
L3 z-side	8.22					
L4	10.1	21 ??	34 ??	8.0??	13??	V_D
L6	20.0	>>30	>>30			V_D
L7	28.0	>>30	>>30	>>30	>>30	V_D
$D\emptyset 90^\circ$	2.70	?	?	?	?	



Achievements (2)

- **If a replacement is required, WG concluded:**
 1. Chip → 0.25 micron of SVX3 architecture
 2. DAQ → New mini-Portcard scheme
 3. Sensors → Single-sided back-to-back rad-hard strips
 4. Modules → Apply L00, CMS concepts and materials
 5. Mechanics → Apply L00, CMS simple ass'ly/support concepts
 6. Material → Studied material budget & its effects: ideas for less
- **Analysis of Run 2a experience: How can we streamline ?**
 - Single-sided silicon
 - Many fewer and more universal components
 - Simple assembly methods
 - Fine pitch signal cables
- **Pixels**
 - Formed a subgroup to study feasibility, cost, schedule for CDF use
 - FPIX chip + ATLAS sensor/module/support concepts
 - More detailed work still required - no show stoppers



Response to PAC

- Our answers to the PAC:

- L00-only replacement could be adequate IF

- Fluences turn out to be at the low end of expectations
- We can live without SVX L0
- SVX L2 can be biased or we can live without it as well

- Any partial replacement of SVXII Layers entails

- Complicated construction issues
- A lengthy shutdown

- A full replacement of SVXII and Layer 00

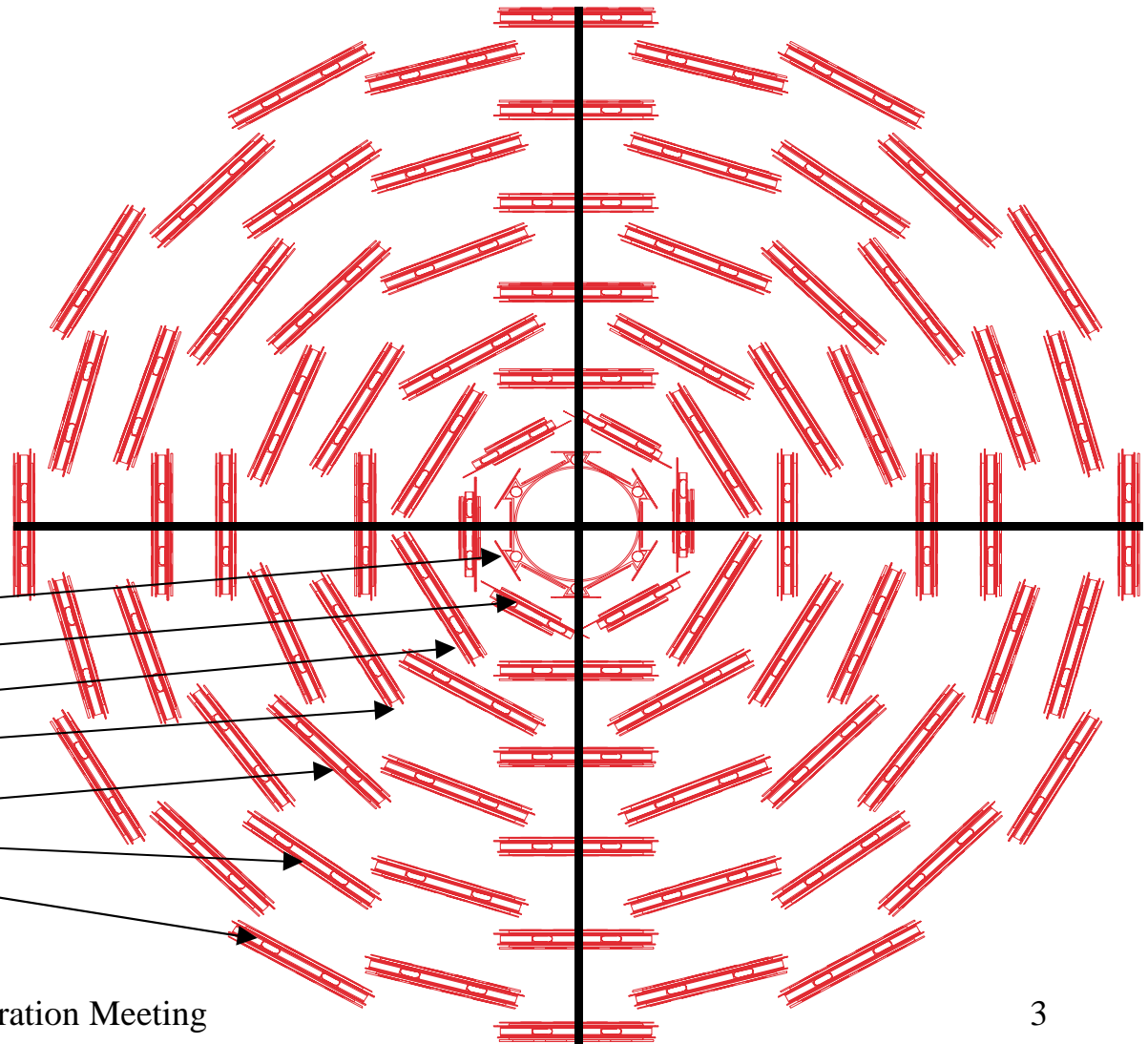
- While it involves more new channels, the Run 2b working group judges this to be an easier and less risky option.
- Involves a much smaller loss of running time than any partial SVXII replacement scheme.
- Could be achieved at reasonable cost and in a reasonable time IF
 - We streamline the design with simple mechanics and a minimum number of different parts
 - Use single-sided silicon
 - We have adequate chips



Run IIB TDR Layout

- ⇒ Double sided staves: axial and stereo sensors
- ⇒ Uniform design for L2-6
- ⇒ 4-fold symmetry for L2-6)
- ⇒ L1 very similar to L2-6
- ⇒ L0 ~ L00 with only 2-chip sensors and supported by beam-pipe

- Layer 0: 12 fold Axial**
- Layer 1: 6 fold Axial-90**
- Layer 2: 6 fold Axial-90**
- Layer 3: 12 fold Axial-90**
- Layer 4: 16 fold Axial-2.5**
- Layer 5: 20 fold Axial-2.5**
- Layer 6: 24 fold Axial -90**



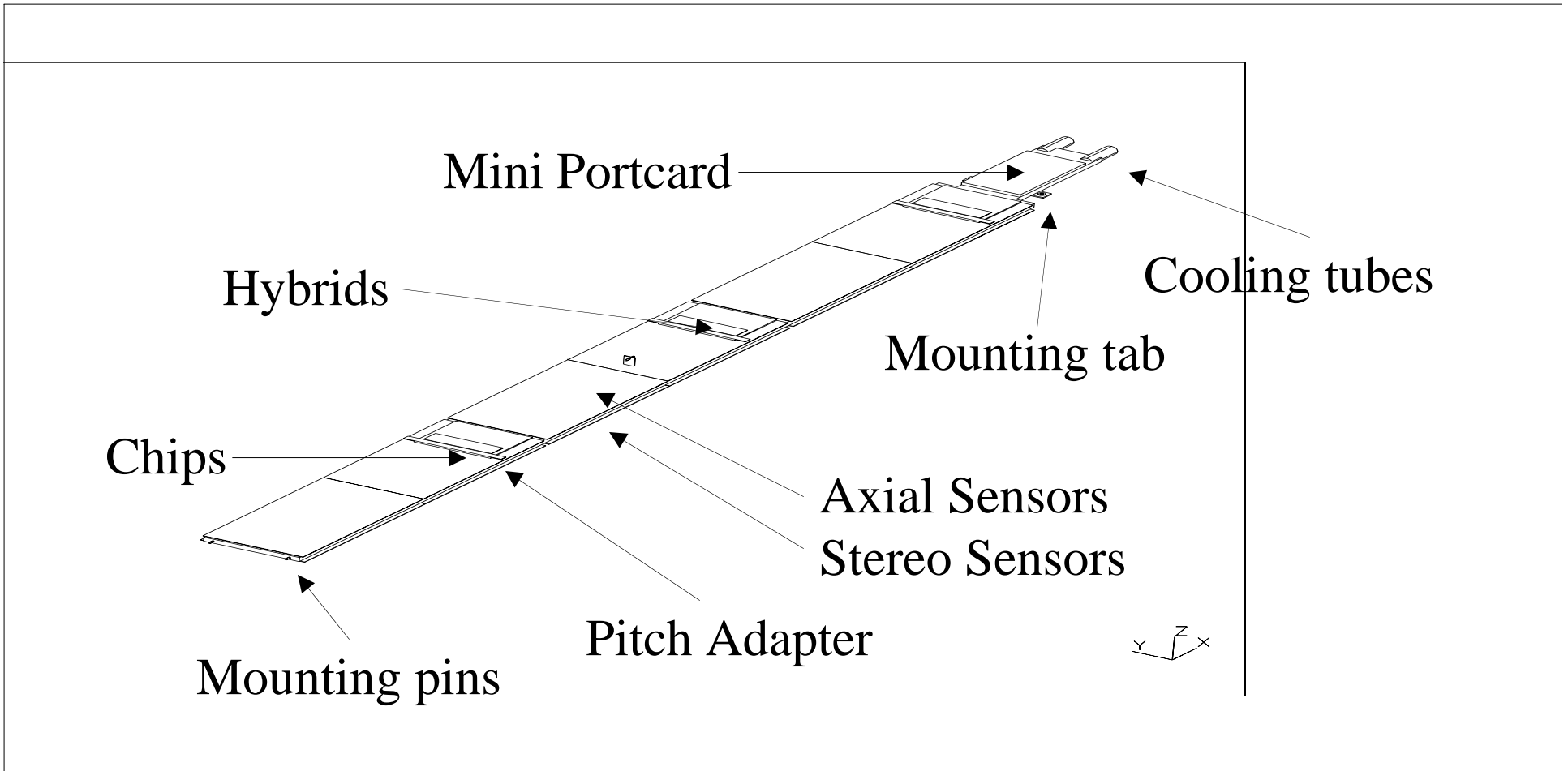


Changes since TDR and Nov. PAC

- Installation date moved to Jan. 05 (3 yrs from now!)
 - ⇒ still only 6m long
- Funding Profile for all M&S for Run2B: 9.1M\$
 - ⇒ Barely fit
 - ⇒ Currently revising cost estimates based on quotes
- **Dropped an inner layer! Now have:**
 - ⇒ Layer 0 – axial (L00 style with fine pitch cables)
 - ⇒ Layers 1,2,5 axial –90
 - ⇒ Layers 3,4 axial-small angle
- Number of readout units/ stave = 1 (TDR had 2 or 3)
 - ⇒ Total number, 252, fits easily within the current DAQ chains (408 available from SVXII and L00)



Run IIB Stave





SVX4 Chip (Dec. 4th)

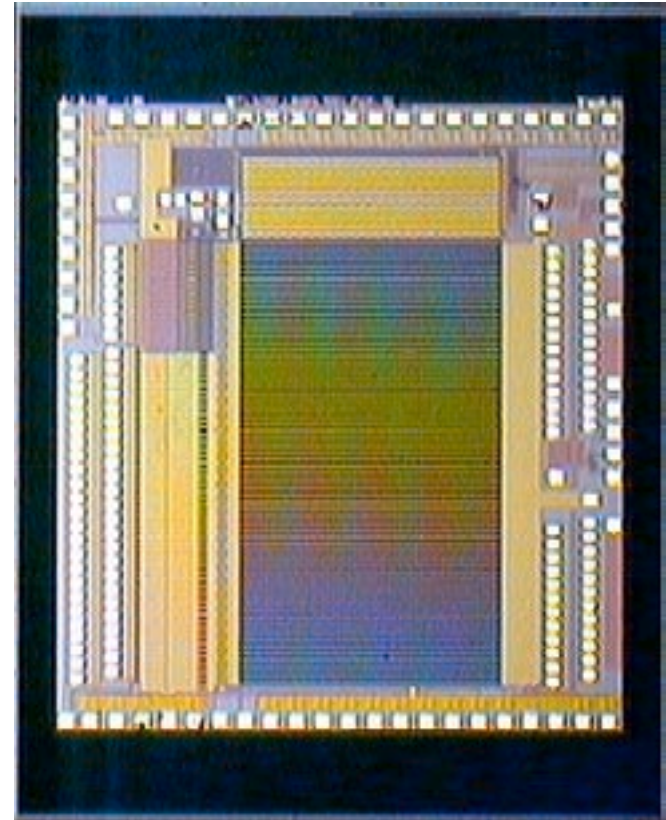
Great progress since last PAC Meeting

- ⇒ Test chips came back in early August – entire frontend (preamp + pipeline) functions!
- ⇒ Chips irradiated to 16 Mrad with Co-60 facility, no changes observed – T. Zimmerman “If some of the other components on the board hadn’t melted, I wouldn’t have believed it was irradiated. ”
- ⇒ S/N 30% better than SVX3
- ⇒ CDF and D0 use same chip

October 22 SVX4 chip review found project is in reasonably good shape

- ⇒ Full chip submission expected Dec. 21st
- ⇒ Will have chips by end Feb. (8 week turn-around)

Most recent estimate is Feb. 15th submission





Milestones

- Major prototyping efforts will be this summer/fall (**Great opportunity for summer visitors!**)
 - ⇒ Start testing in June with chips and hybrids
 - ⇒ Sensor testing and modules in July
 - ⇒ **First electrical modules and staves in October 02!**
 - ⇒ Pre-production June 03
 - ⇒ Production Oct 03- August 04 (rate 1 stave/day)
 - ⇒ **Assembly and testing Sept. 04-Jan.05**
- End game
 - ⇒ Run2a ends Jan.1 05
 - ⇒ ISL ready for Run2b SVX Mid March
 - ⇒ We have 2.5 months of float at end of schedule – may change as we update with true submission dates.



Run IIB Silicon Upgrade: UCD Role

- ❑ Test hybrids with new SVX4 readout chips
 - *Set up test stand at UCD*
 - *Linux system with PCI interface, oscilloscope, etc.*
 - *Work with LBL SVX4 chip experts to test new chips*
- ❑ Stave production: > 1200 Hybrids must undergo "burn-in"
 - *Design and build 64-hybrid burn-in system at UCD*
 - *Process all hybrids at UCD prior to assembly at FNAL*
- ❑ Schedule
 - *SVX4 chip to be submitted this month*
 - *Components to test in late May*
 - *SVX4 pieces available for burn-in in June*
 - *Assemble prototype stave mid October*
 - *Preproduction early 2003*
 - *Production mid 2003 through mid 2004*



Conclusions

- Highly modular and buildable design for the Run IIB Silicon Detector
- Maintains the tracking capability of the CDF detector
- Total mass in tracking volume is reduced
- DAQ simplified, active components are more accessible
- Design has been simplified since TDR by dropping a layer.
- Optimization of Layer 1 design is in progress
- Design and prototyping efforts are underway for outer layer components
- Finding the Higgs will be difficult, we need as much b-tagging efficiency and redundancy as possible.