Hybrid Burn-in Hardware for Preproduction

Run IIb Upgrade Workshop
Davis
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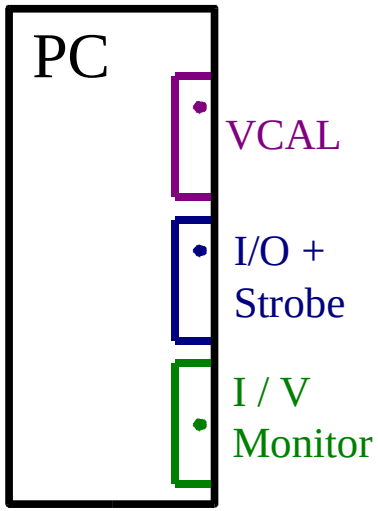
Outline

- Hardware requirements for preproduction
- Challenges of running at 50 MHz
- Prototype Multiplex Scrambler (MPX) modifications for preproduction
- Prototype Pattern (PATT) board modifications for preproduction
- Conclusions

Hardware for (Pre)production

Linux PC:

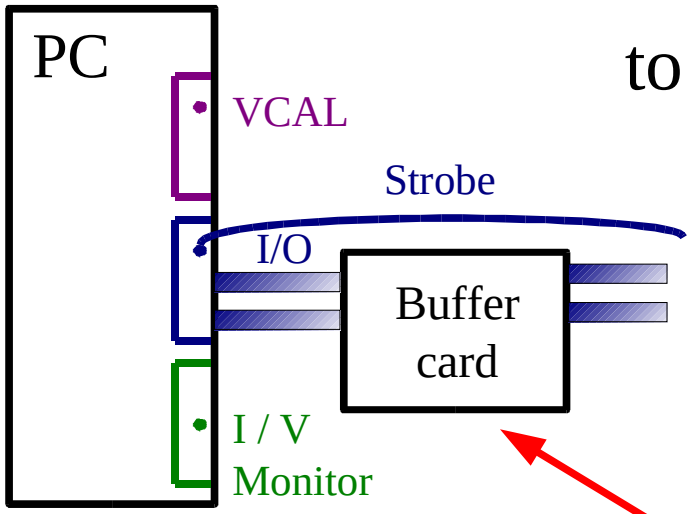
- Control & read out burn-in stand
- Runs “hybmon” software
- 3 PCI cards:
  - I/O – control & read out, Strobe line
  - Current and voltage monitoring (ADC)
  - VCAL (DAC)

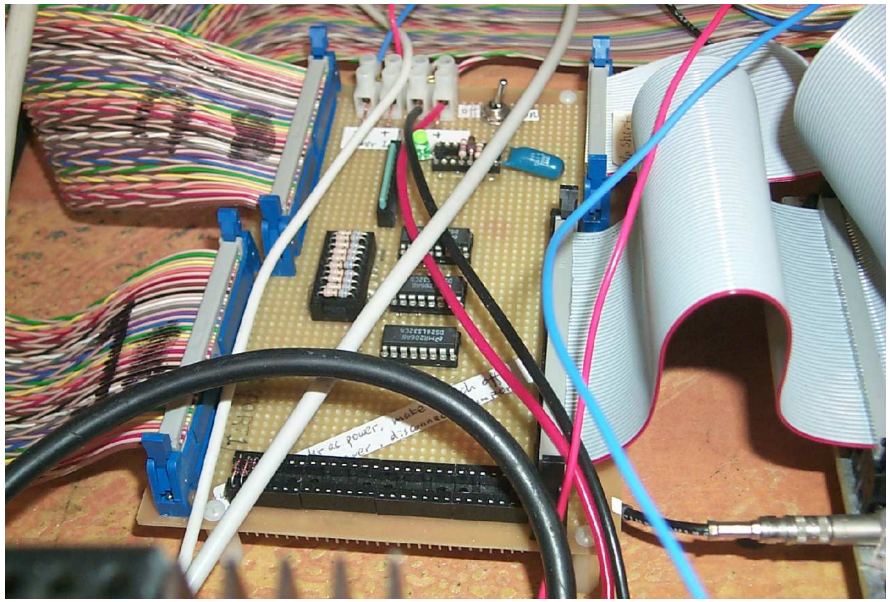


Hardware for (Pre)production

Buffer card:

- Provides pass-through for input pattern and control lines
- Converts returning data from differential to single-ended format





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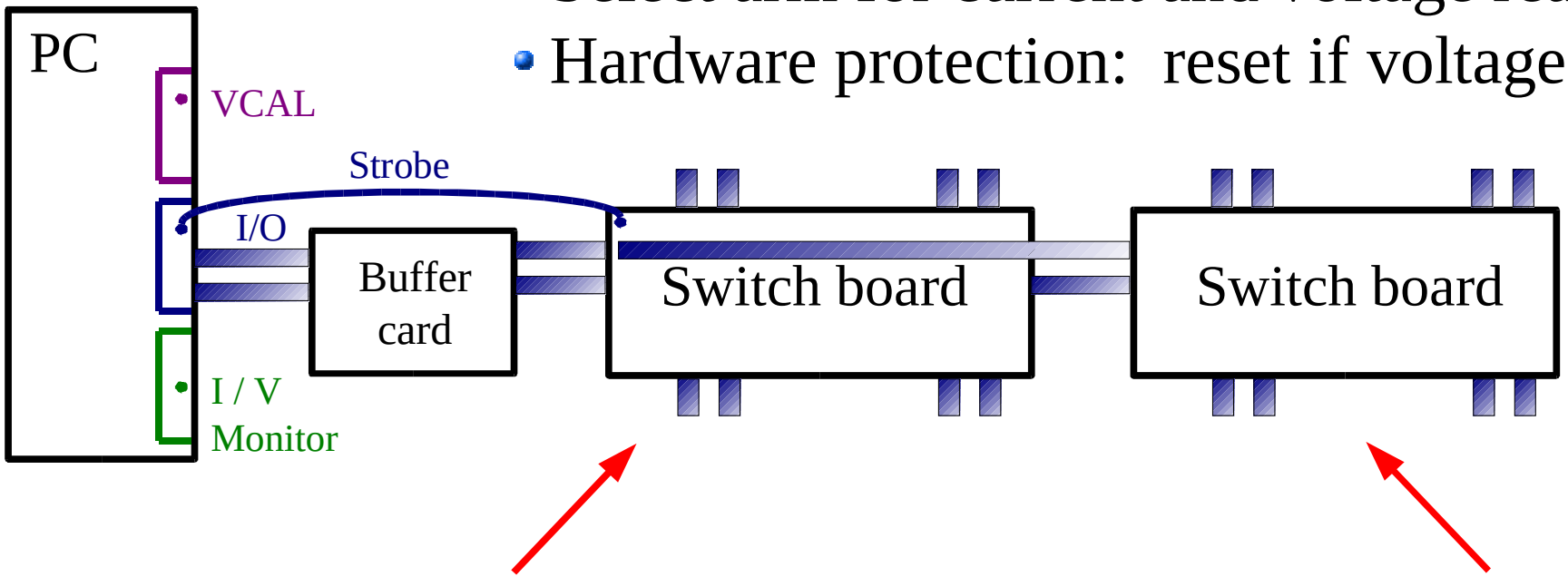
Hardware for (Pre)production

Switch board:

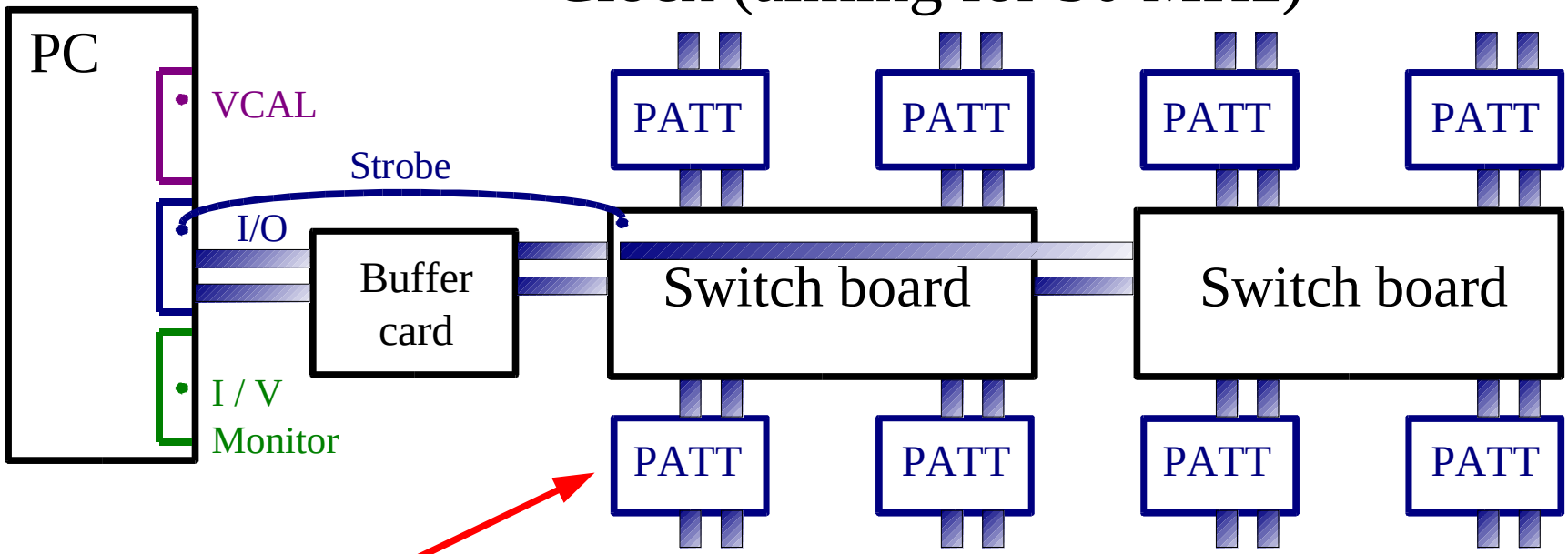
- Provide power switching and I/O routing to and from each of the 8 arms
- Select arm for current and voltage reading
- Hardware protection: reset if voltage drop

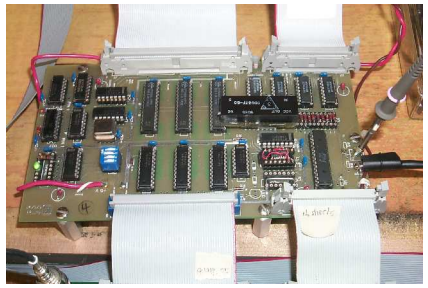


Hardware for (Pre)production

Pattern board: (PATT)

- FIFOs for sending patterns to hybrids
- FIFOs for receiving data from hybrids
- Clock (aiming for 50 MHz)





- Timing needed for init./control, readout
- Logic for selecting “Data Valid” or “Pri. Out” for 9th bus line from hybrid

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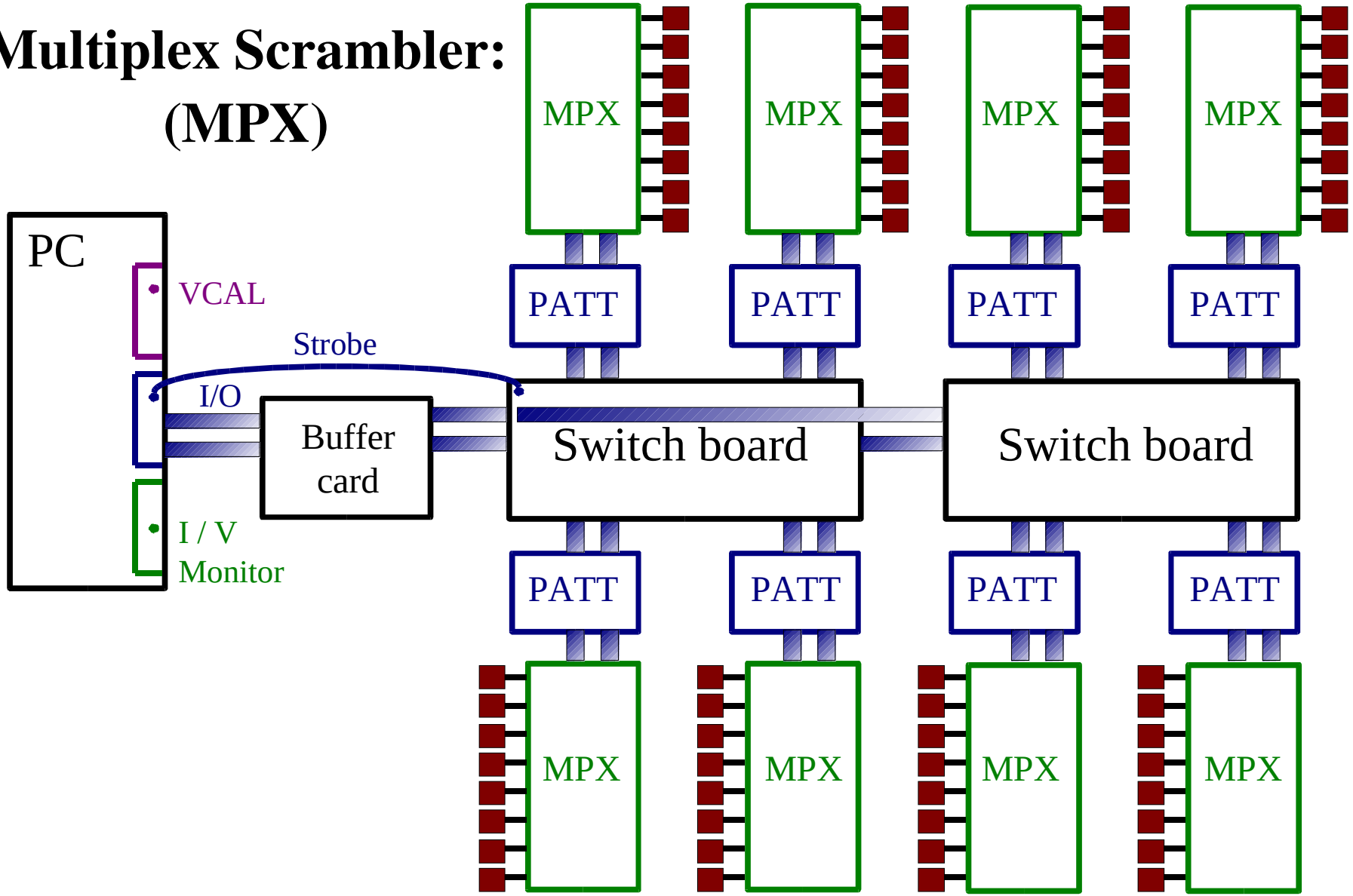
New Multiplex Scrambler Board!

MPX:

- Distributes initialization, pattern, and control to 8 hybrids (sends to all 8 at once)
- Distributes analog and digital voltage to hybrids (either all on or all off for a given MPX)
- Selects among hybrids for readout
- Selects among hybrids for current and voltage monitor

Hardware for (Pre)production

Multiplex Scrambler: (MPX)



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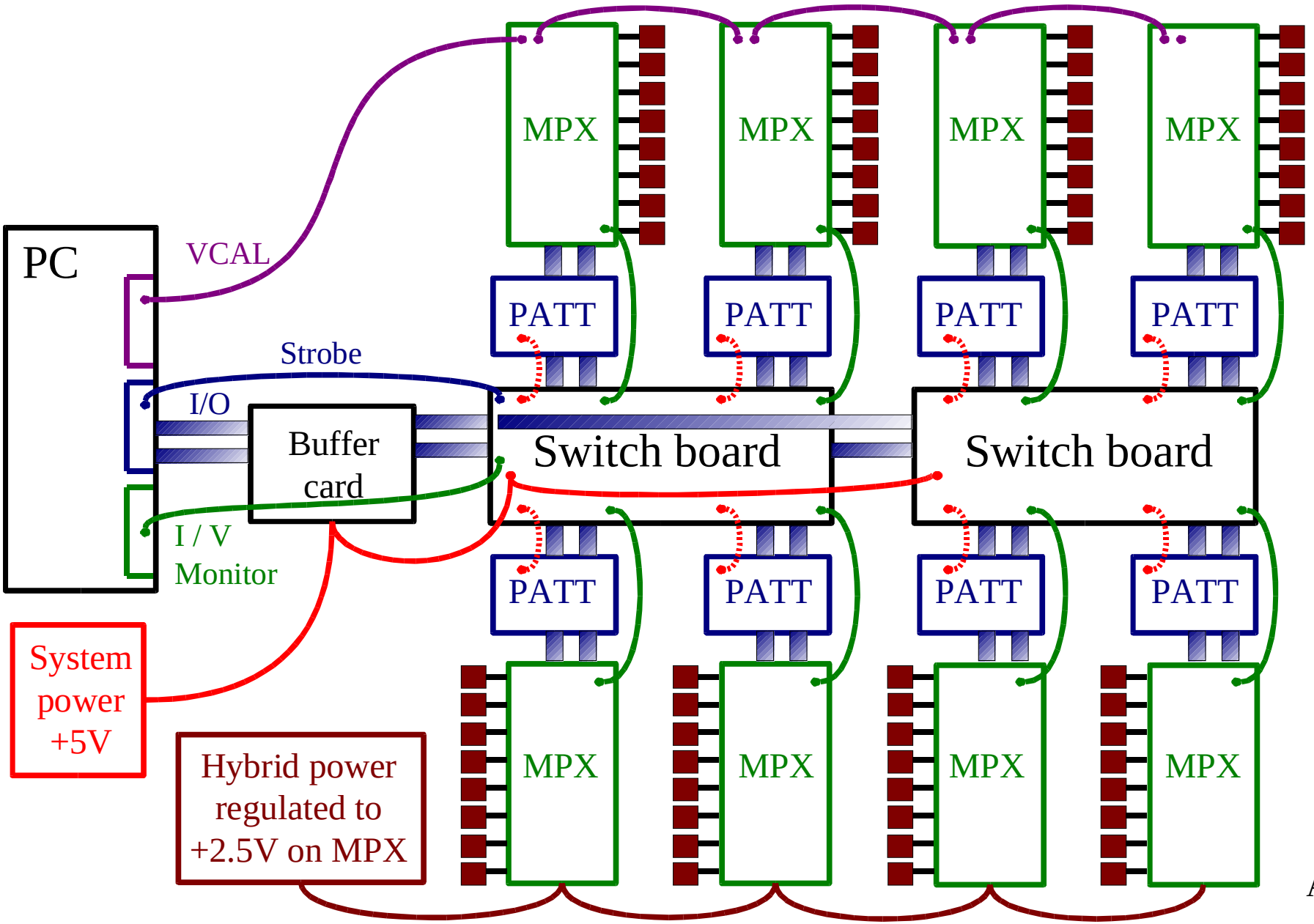
Hardware for (Pre)production



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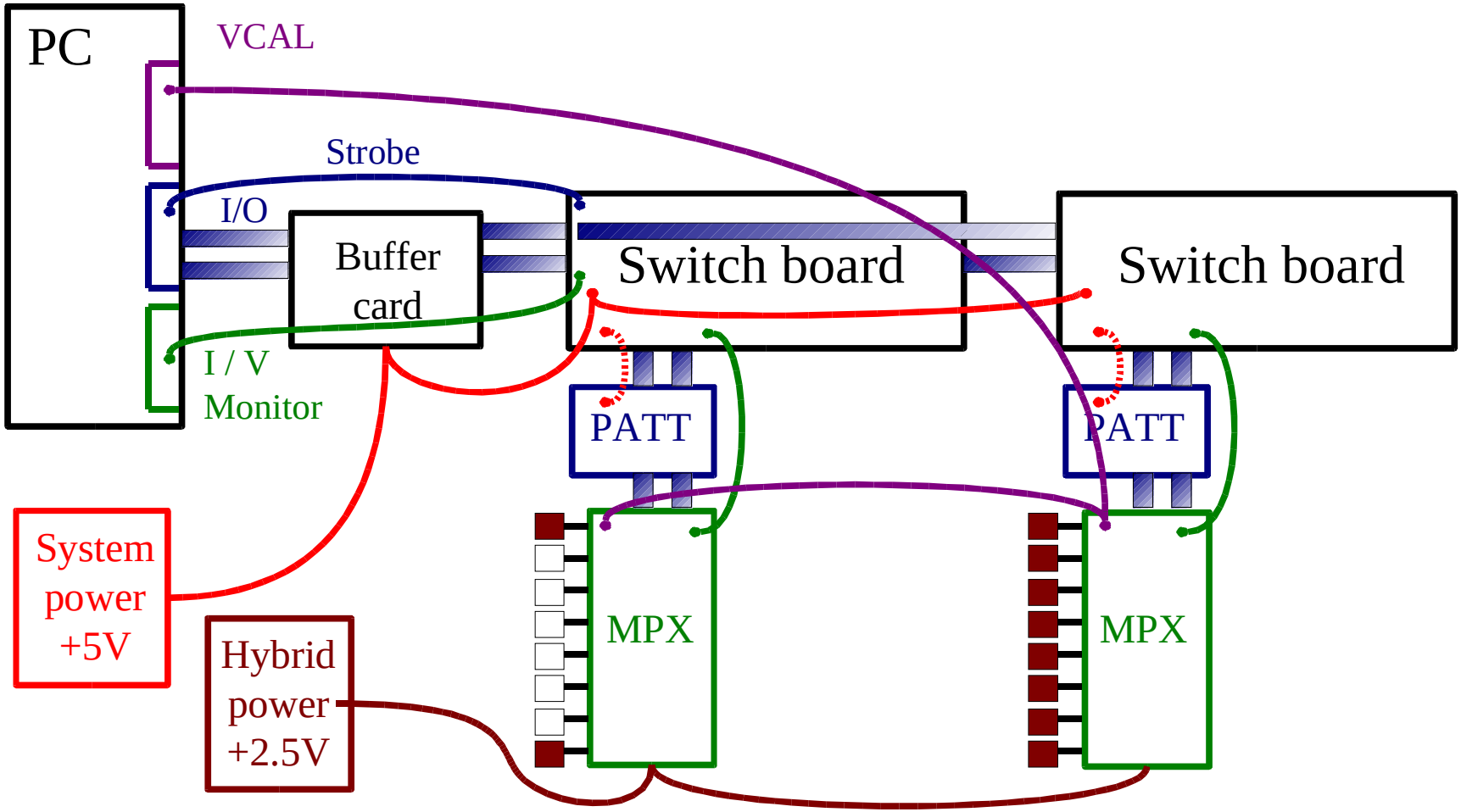
For Preproduction

- Prototypes will be equipped to burn-in 10 to 16 hybrids
- Tests complex features of hardware
- Keeps up with preproduction



Challenges of Running at 50 MHz

- Clock skew between two ends of MPX
  - Additional 1.5 ns delay in arrival time at PATT FIFO of output data from each of the successive 8 ports of MPX
    $\Rightarrow$ 10.5 ns difference between port 1 and port 8
  - Compare this with the store period of 20 ns (50 Mhz)
- "bit9" selection on PATT board adds additional delay
  - There are 10 bus lines, but only 9 PATT board FIFO bits
  - "bit9" carries either "data valid" or "priority out"
  - The logic on the PATT board that selects between the two adds additional delay with respect to the other 8 bus lines
- Both effects have been reduced through modifications, but running at 50 MHz is a *new* challenge

MPX Modifications for Preproduction

- Inverted bits found in two of the input lines (fixed in software)
- Termination added to input and output bus lines
- Driver chips added to output bus lines
- Lowest driver current setting gives poor differential signal (an item for discussion)
- Swaps between connections to pins of current and voltage Monitoring chips (fixed on MPX board)
- Swap between AVDD and DVDD connections (fixed)
- Delay added to back-end clock as sent to ports 1-4
  - Delays the readout of ports 1-4 to match the readout of ports 5-8
  - Reduced the clock skew to two sub-groups

PATT board Modifications for Preproduction

- Clock signal, as used for FIFO store, cleaned up
  (diodes and resistors added to PATT board)
- More direct ground paths established
- Circuit that selects bit9 has been sped up
  (from ~12 ns to ~5 ns)

Conclusions

- Plan is to run at 50 MHz
  - There have been challenges, but we are on target
- Prototyping concept has been a success
  - Problems have been identified and fixed
- Prototype MPX board has undergone modifications
  - In preparation for preproduction
  - Changes will be included in layout for next (production?) version
- PATT board is ready for submission
  - Need for more boards has given an opportunity to improve them
- Hardware for preproduction is on hand, with ongoing work on MPX to allow for preproduction burn-in of 10-16 hybrids simultaneously