Deadtimeless stave performance/ bus cable design

Marc Weber 7/29/03

What is the problem ?

- Chip operates in deadtime-less mode: can acquire data while reading out or digitizing + stave bus cable traces run directly under sensor => this can yield to **systematic pedestal shifts**

Why is this bad ?

- have to sparsify: only channels with ADC > threshold are read out => if pedestal shifts up, we read out **fake hits** and get VERY **big events**; if pedestal shifts down, we may push a real hit below threshold and are **inefficient**

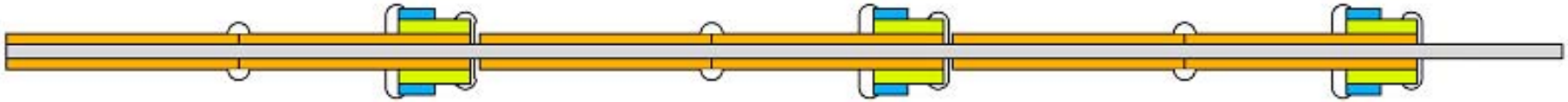
What‘s the mechanism for the pedestal shifts ?

- It is not the chips or hybrids (alone)

- chip pedestal in deadtimeless mode is **flat** for all practical purposes
- pedestal shifts are a **system** property: need chips (hybrids), bus cable and sensor to get them...

How does the system look mechanically ?

(concentrate on salient features ...)



- Chips on hybrids (to state the obvious)
- hybrids on sensors (NOT standard, but is OK)
- **sensors on bus cable**
  - crucial feature, quite unusual, attractive mechanically
- bus cable has aluminum shield layer separating copper traces and sensor backplane

How does the system look electrically ?

This is not a simple electrical system !

- **Digital ground = analog ground** on each hybrid
  - required by chip architecture, there is no choice
- **HV ground = analog ground** on each hybrid
- aluminum shield is **„grounded“**
  - can choose one common shield or three shields at corresponding hybrid
  - which ground should be connected ?

System is also fairly sensitive

- voltage shifts on HV or HGND look like integrated charge due to a real particle
- example: Cdet = 10 pF, Qmip = 4 fC => even shifts in the order of millivolts can be annoying !

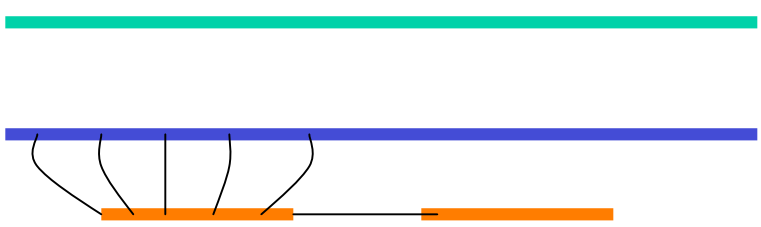
How could these voltage changes happen ?

- **conductive** interference (ground loops, common impedence effects ...)
- **capacitive** (electric) interference
- **inductive** (magnetic) interference
- (electromagnetic radiation)
- the first 3 effects all seem to matter in our system

Examples: Capacitive coupling

- $Z = -i/\omega C$ => large C and large frequencies ω both lead to strong coupling and thus big pedestal shifts
- e.g. PRD1 with ~ 4 ns risetime is dangerous, ditto CHMODE, BEMODE etc.
- Example: see plot with floating shield and with artificial chmode signal placed somewhere during readout
- Why are we sure that this is capacitive coupling ?
  - chmode has no effect on chip without BE/FEMODE change
  - effect goes away with grounded shield
  - don`t see similar spikes for differential signals

Canconical way to avoid capacitive coupling is by shielding/grounding



sensor

Alu shield (grounded !)

copper traces

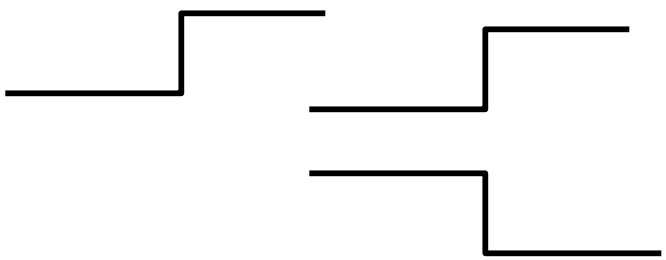
- Field lines end on shield => no coupling to sensor
- measurement: stave with grounded aluminum shield
- Capacitive coupling is nearly completely gone
- to be discussed later: what is best ground; what happens if ground moves ?

Other methods that don‘t work

- reduce **trace width** and thus C; however cannot go much less than 3 mils
- reduce **risetime**; not practical for many reasons
- change cable thickness; little change in C because field lines still have to end somewhere...
- reduce signal levels

Other methods that would work

- **differential lines** rather than single-ended ones
  - requires transceiver on hybrid and hybrid redesign + bus cable redesign
  - fortunately we don‘t have to do this
- **optimize pattern**: eg. have chmode rising and falling edge within same bucket !



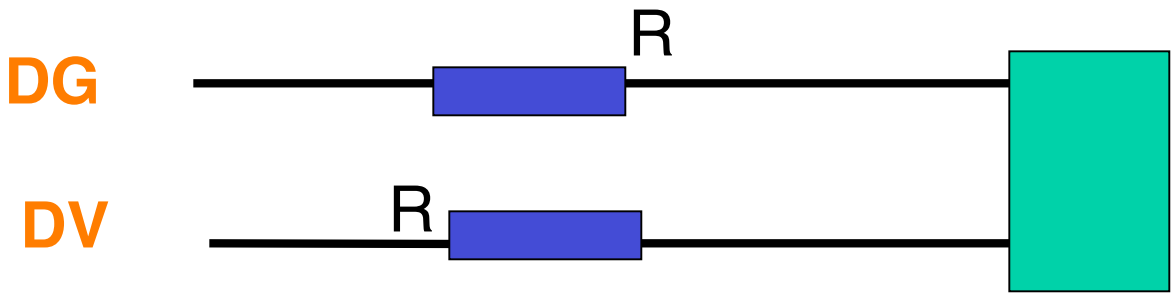
Single -ended

Differential

Other methods that would work (cont'd)

- Subsequent charge injections of different polariy cancel within the same bucket
- method works for CHMODE but not for PRD1, PRD2, CAL/SR, FEMODE, BEMODE
  - only PRD1, FEMODE, BEMODE are a problem anyhow
  - compensation happens always for L1A too

Examples: Conductive interference



- chip power consumption can vary significantly eg. by switching on/off drivers or changing modes
- ♣ ΔI x R = Δ U => change of DG/AG/HG ground level and effective charge injection into preamp

possible cures

- a) **decoupling**: charge is quickly provided by decoupling caps, recharging occurs over much longer time scales (bulk caps) => smaller effects

Conductive interference (cont‘d)

- lower R => less voltage drop

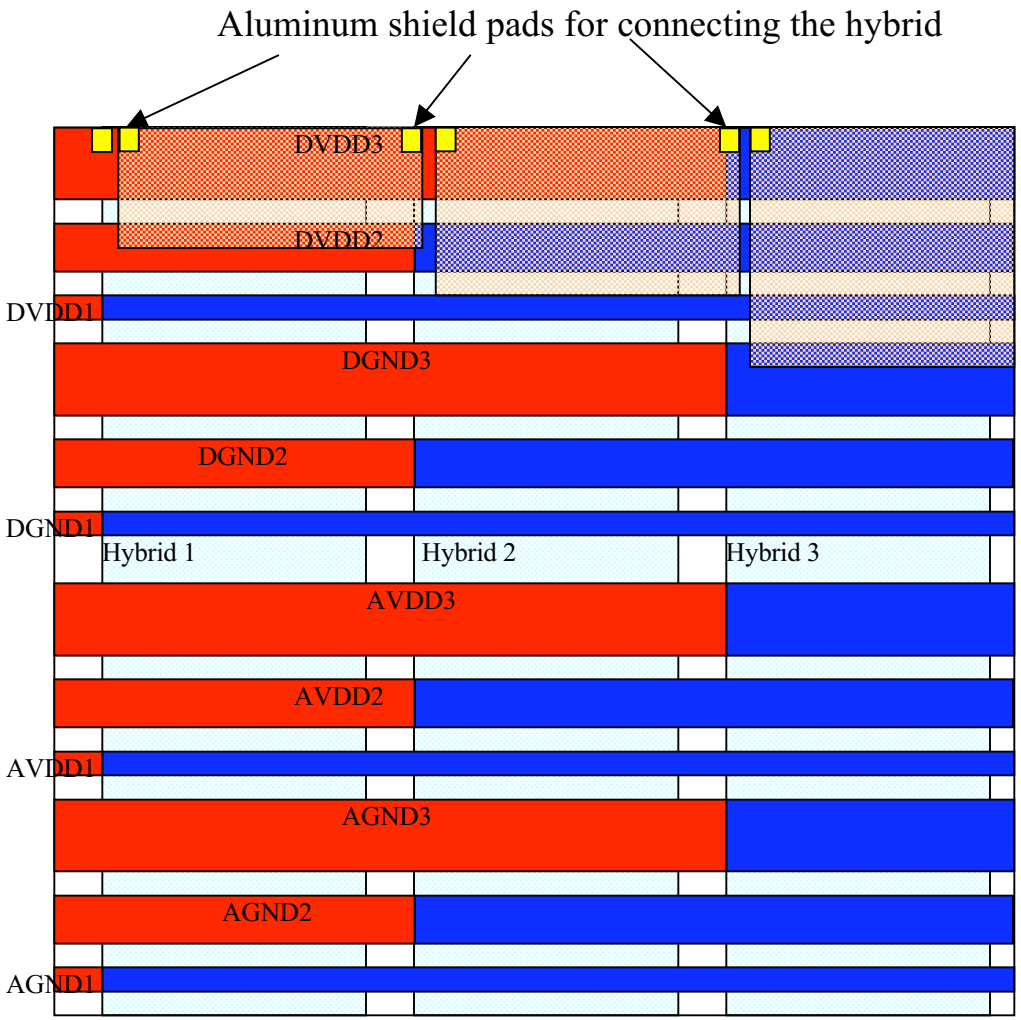
How ?

- Thicker copper traces: eg. double _ oz of copper / ft^2 (18 um thickness) to 1 oz...
- however, copper is 6% of RL of a stave => don‘t go there
- remaining solution: wider power traces

- (-> old/ new cable plots)

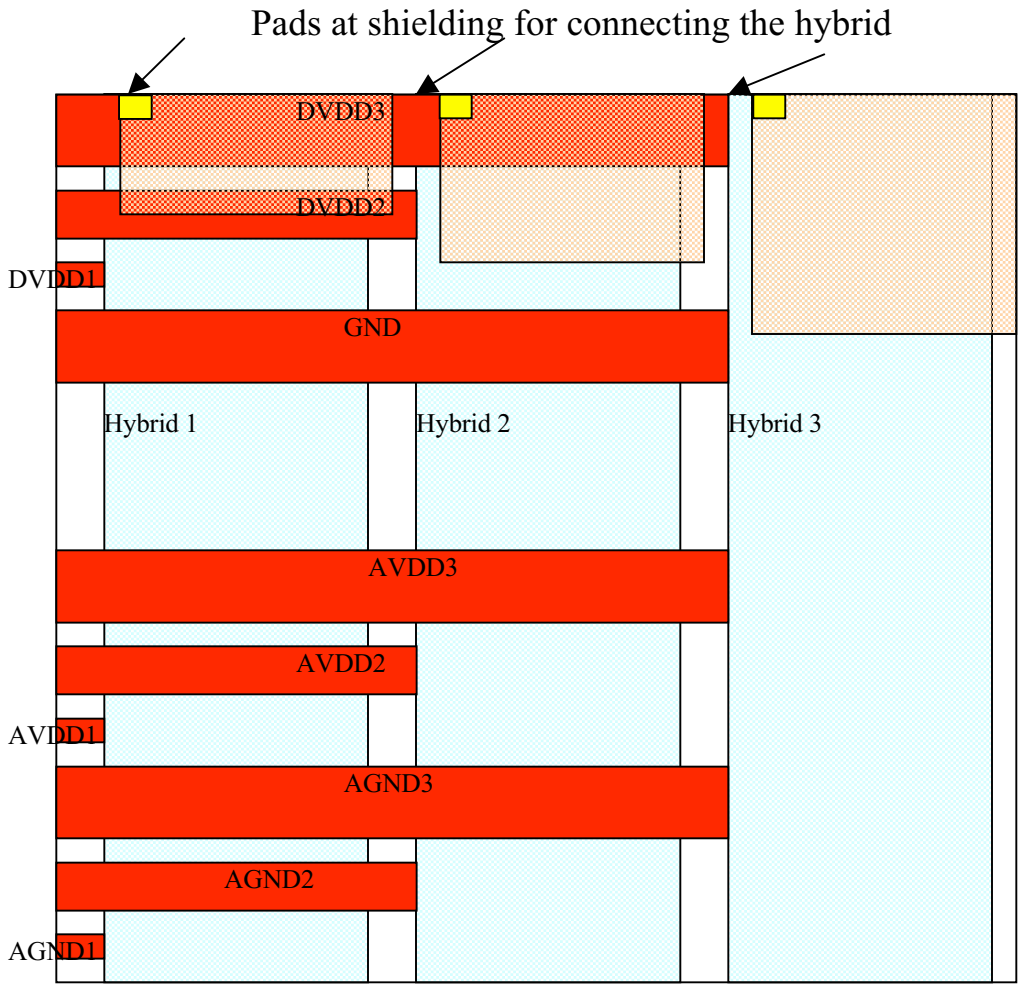
Old cable:

- AV 1-3, AG 1-3, DG 1-3, DV 1-3 all separate
- traces extend over full length of cable



New cable:

- DG 1-3 combined
- traces don't extend over full length of cable, remaining space used to widen other lines

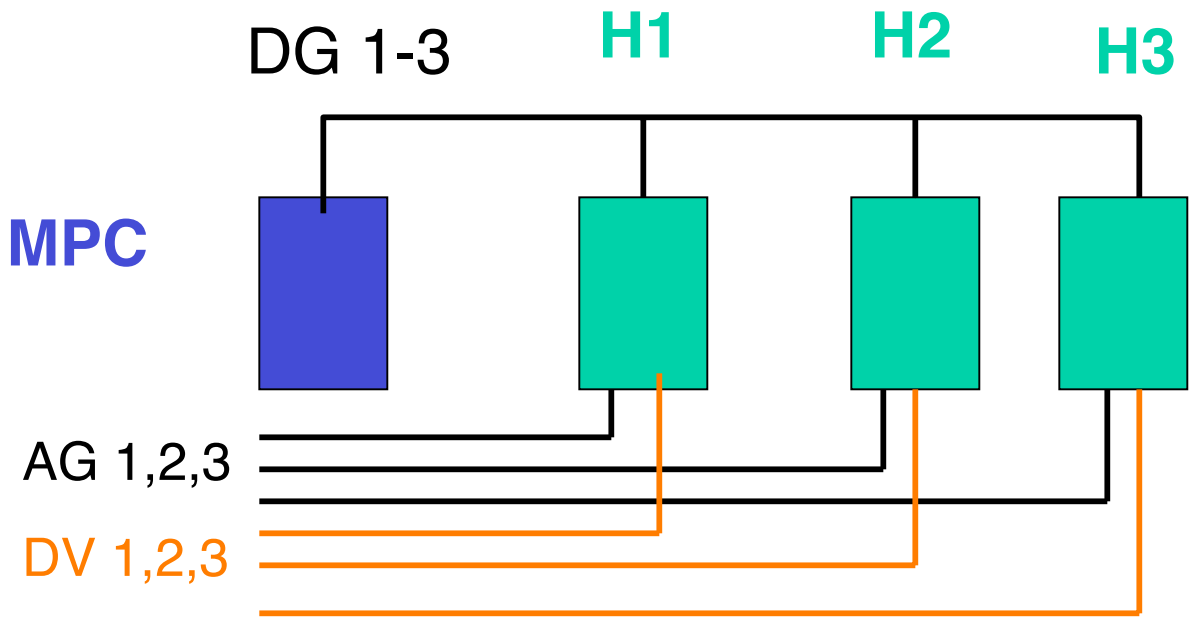


Decrease R

- wider power traces also mean better capacitive coupling to shield
- should be OK since shield is grounded and we have strong decoupling caps on power
- see big improvement when reducing R by bonding AG 1-3, DG 1-3 together on old cable
- Why did we not combine AG 1-3 together too on new cable ?

Ground loops

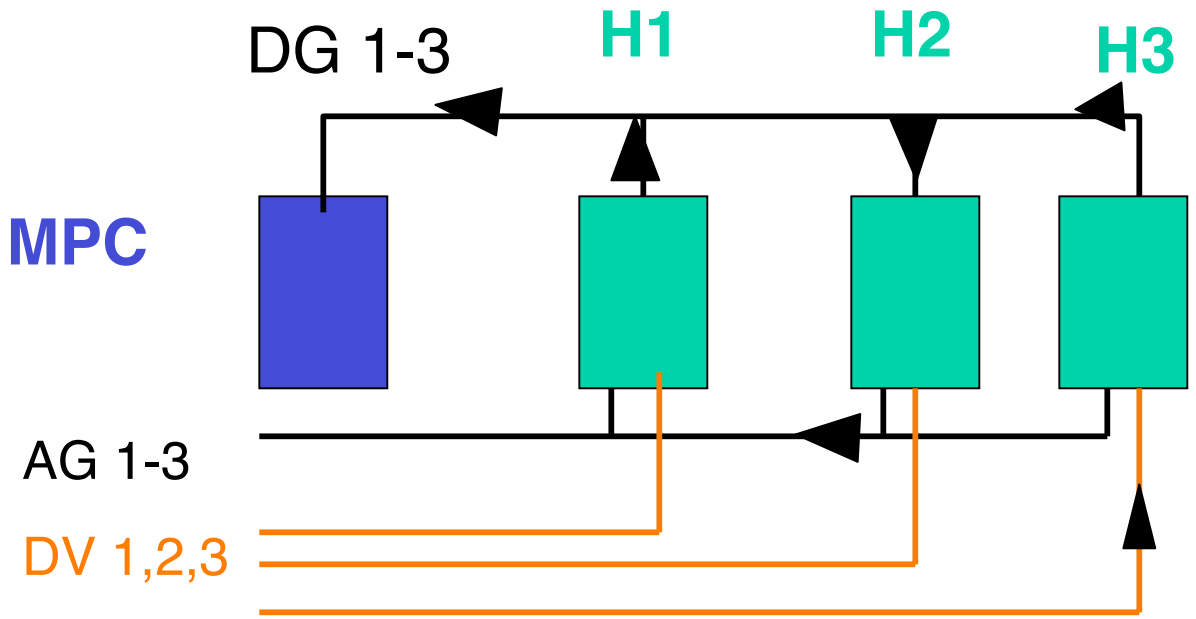
new cable with DG 1-3



=> `no' ground loops

Ground loops

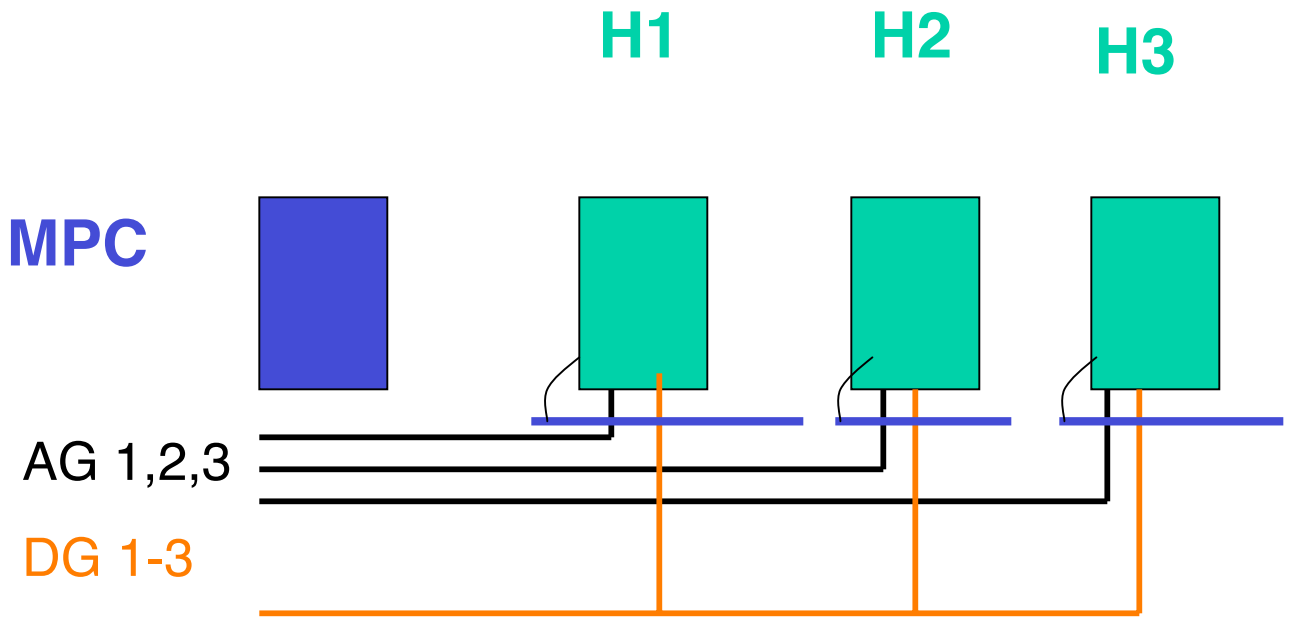
a cable with both DG 1-3 and AG 1-3 combined



- many ground loops – since DG and AG are connected on hybrids
- => current change in digital can influence any hybrid
- better to avoid this

Ground loops

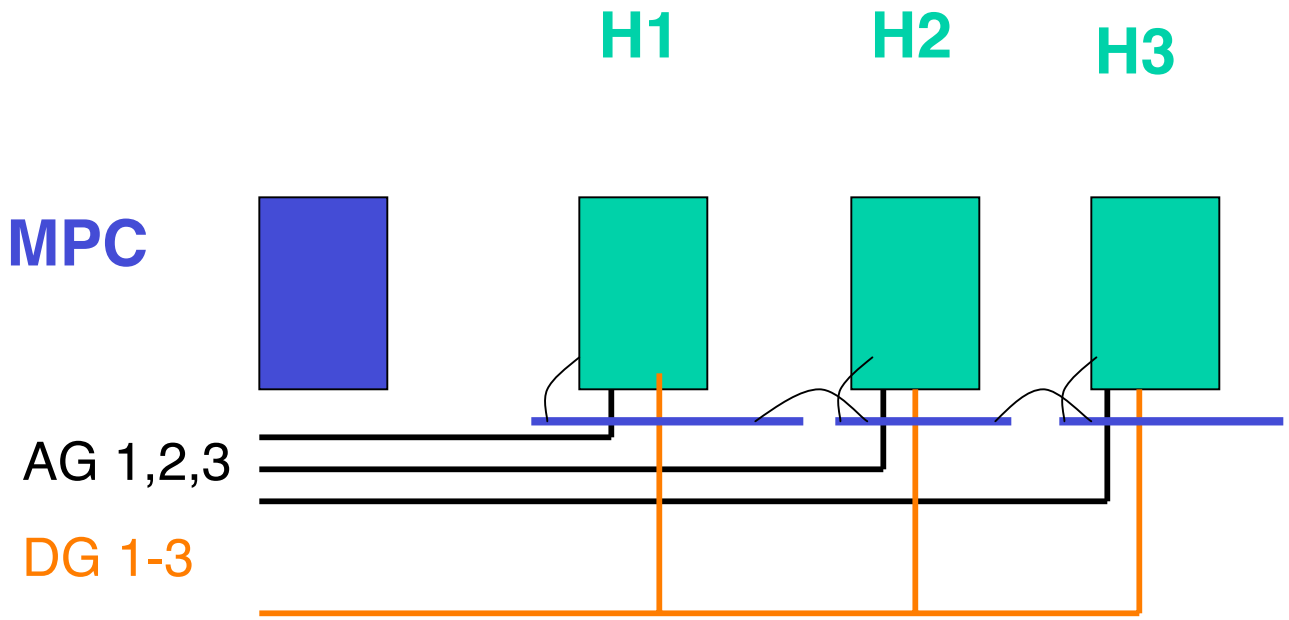
Why have a local shield ?



- Local shield: no current through shield, local ground

Ground loops

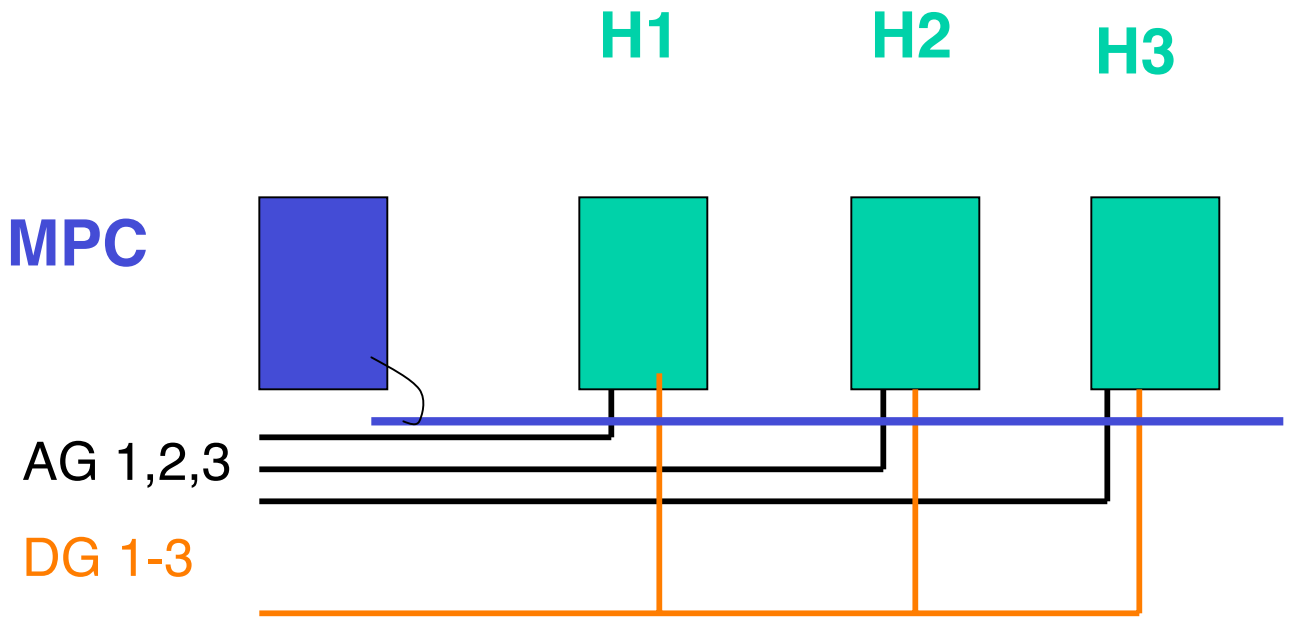
alternative 1: one big shield grounded locally (`hybrid' scheme)



- Many ground loops, current will flow through shield

Ground loops

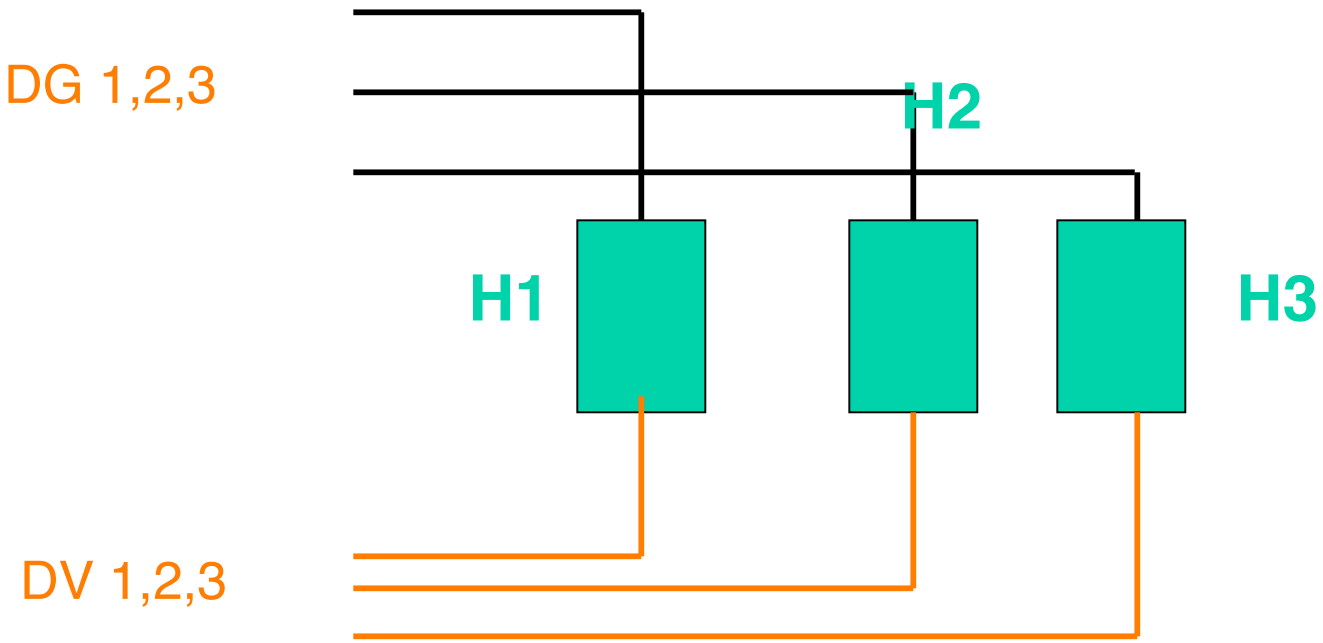
alternative 2: one big shield grounded at MPC



- `no' ground loops but measured to give worse performance

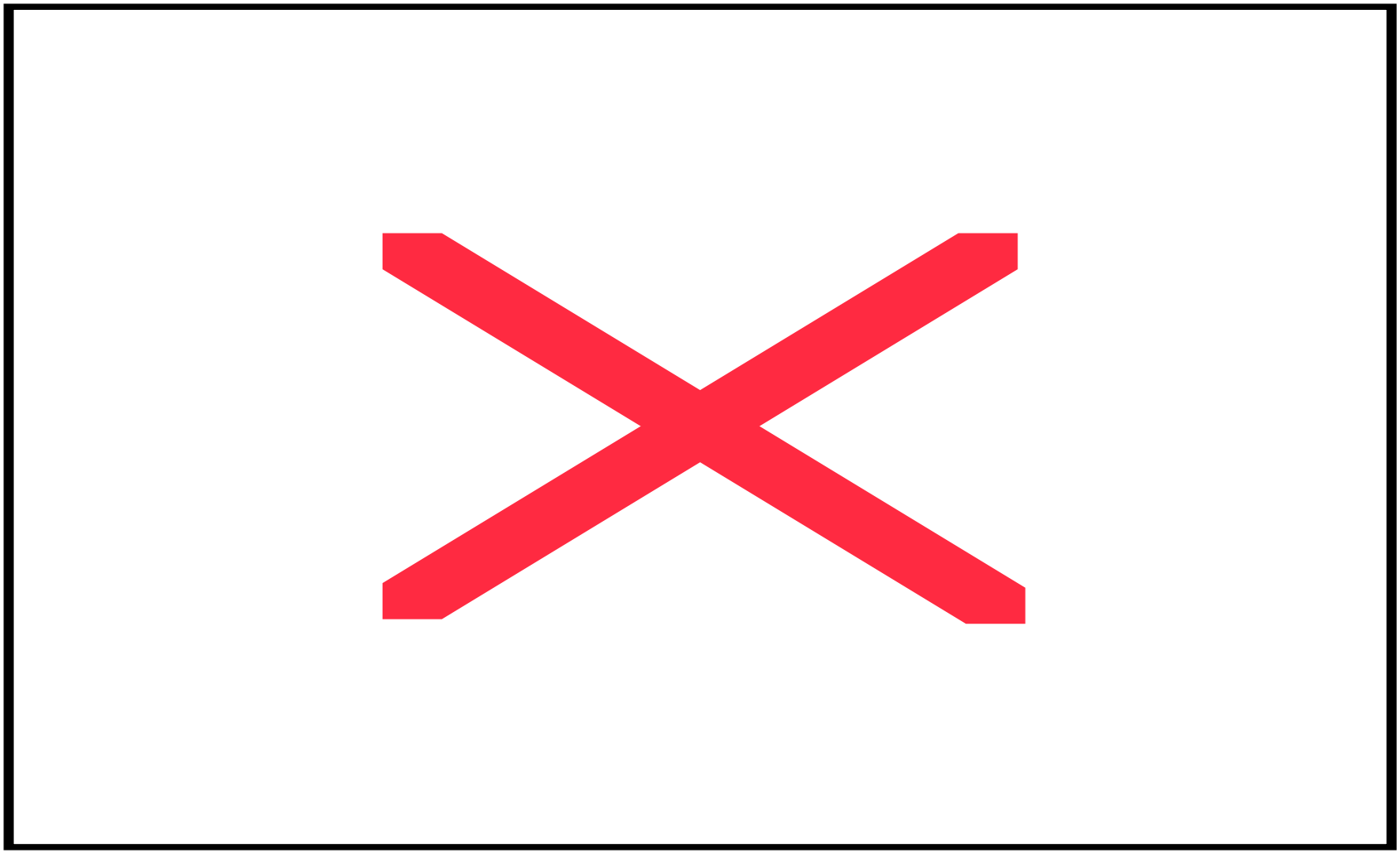
Magnetic interference

Started to design a **cable** but got a **transformer** instead



- overlapping loops => digital current change on hybrid 1 will induce noise voltage in hybrid 2
- set of function generator and scope to measure mutual inductance on bus cable

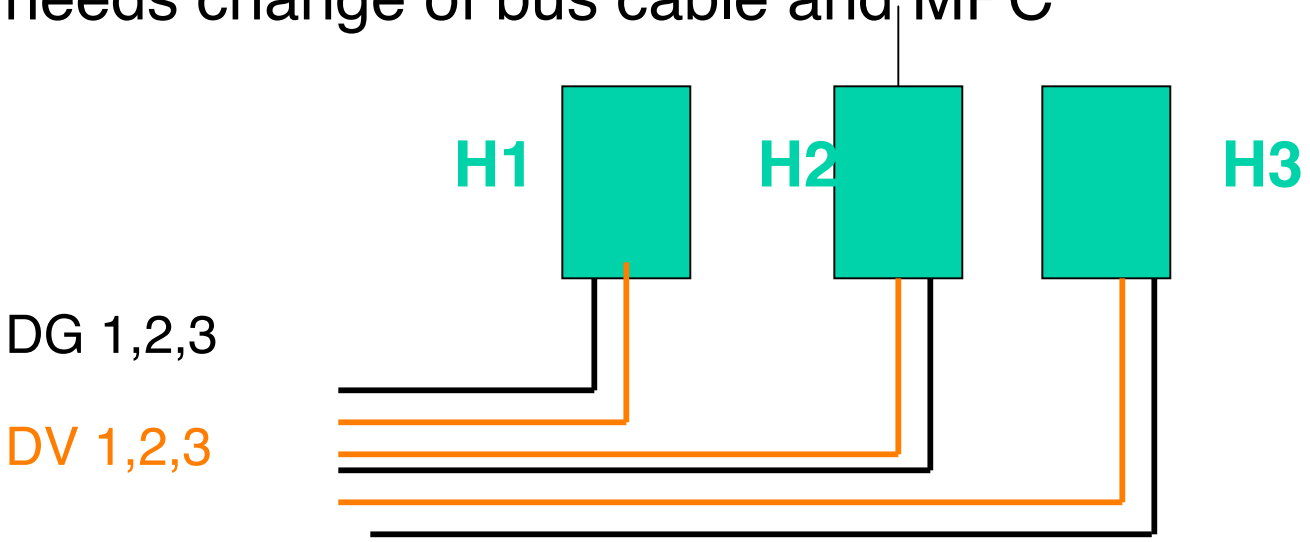
Inductance tests on bus cable (Mika)



- still very preliminary, complex frequency dependence …

Magnetic interference (cont‘d)

- it’s still unclear how important this effect is
- could have avoided it by a different geometry (no overlap)
- needs change of bus cable and MPC



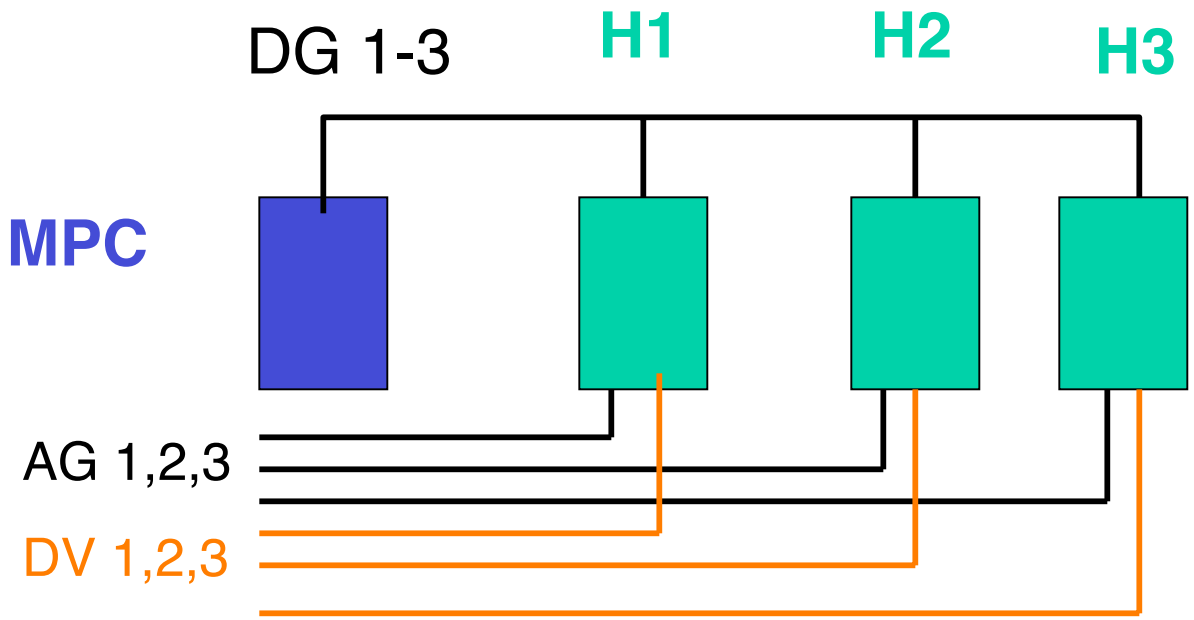
Summary

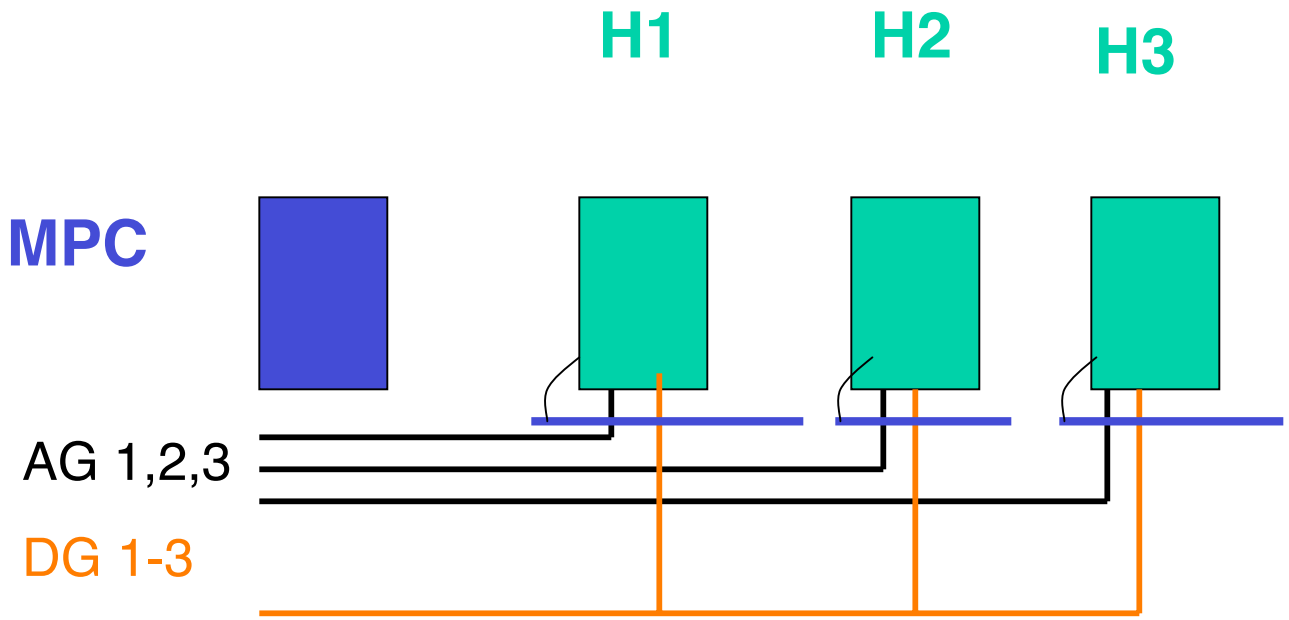
- have learned a lot in last few months recently !
- thanks to Lu, Sergio and Mika

- Stave deadtime-less performance is fairly good already
  => Validation of stave concept
- Further improvement is possible with new cable

Still to do:

- understand priority structures and inductance effects better
- understand 396 ns patterns
- measure performance of stave with new cable


DG 1-3
H1
H2
H3
MPC
AG 1,2,3
DV 1,2,3


H1
H2
H3
MPC
AG 1,2,3
DG 1-3