UC Davis

and

CDF Run 2b Upgrade

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Grad Student Seminar

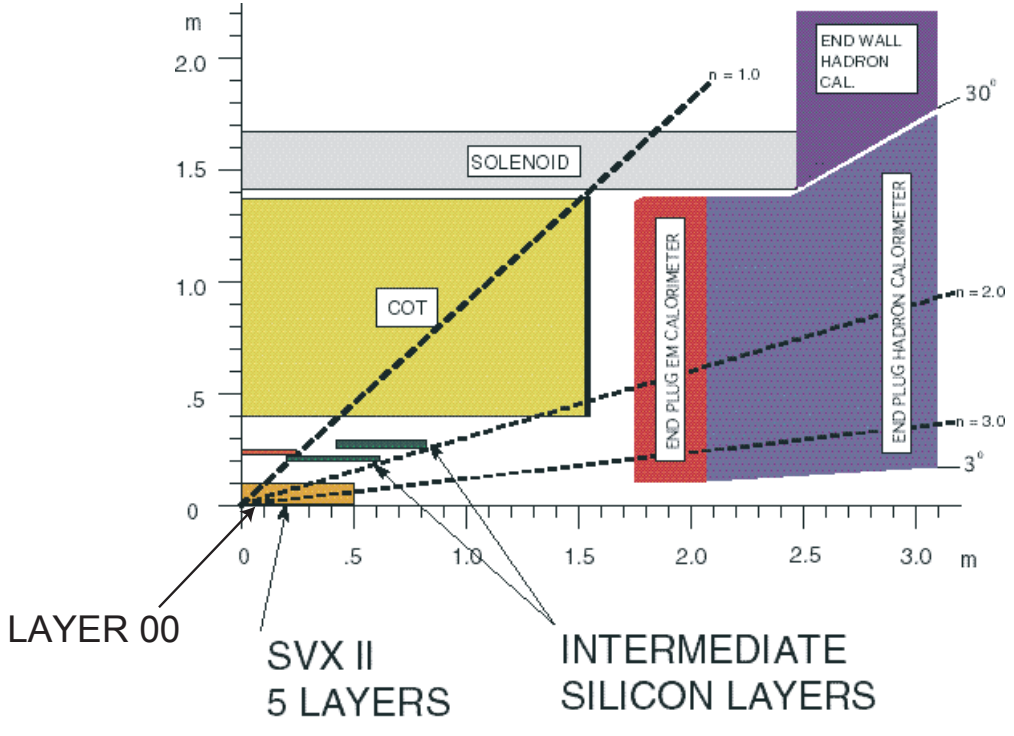
January 15, 2003

Outline

- *Background:* UC Davis and Run 2a upgrade
- Tevatron luminosity upgrade for Higgs *(and other)* searches: **Run 2b**
  - Tevatron is energy frontier
  - Targeted detector upgrades imperative for high mass physics searches
- Run 2b silicon vertex detector (SVX) upgrade
  - General overview and schedule
  - R&D work at UC Davis
  - Major task: "burn-in" and debugging of all the SVX hybrids for Run 2b (over 1000) at UC Davis
  - Description of UC Davis plans, activities, requirements and schedule

Background: UC Davis and Run 2a Upgrade

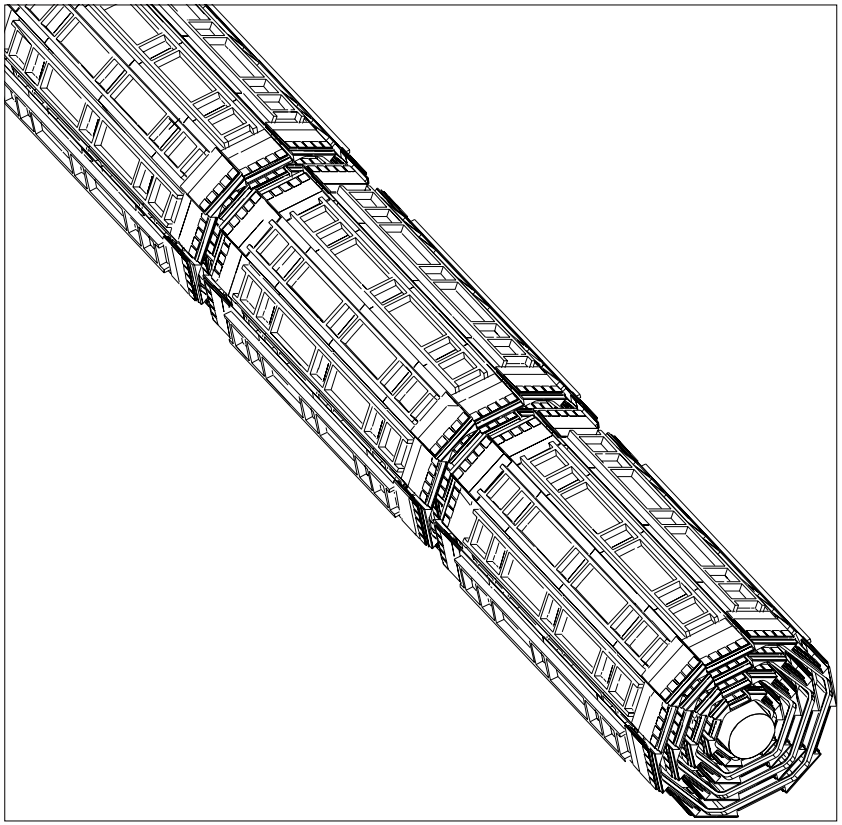
- ISL and Layer 00 at Fermilab: hybrid burn-in, assembly
- ISL cable interconnect electronic design
- Readout hybrid testing at LBL
- Studies at UC Davis cyclotron
  - SVX3 SEU cross section measurement
  - Radiation damage of silicon strip, readout components

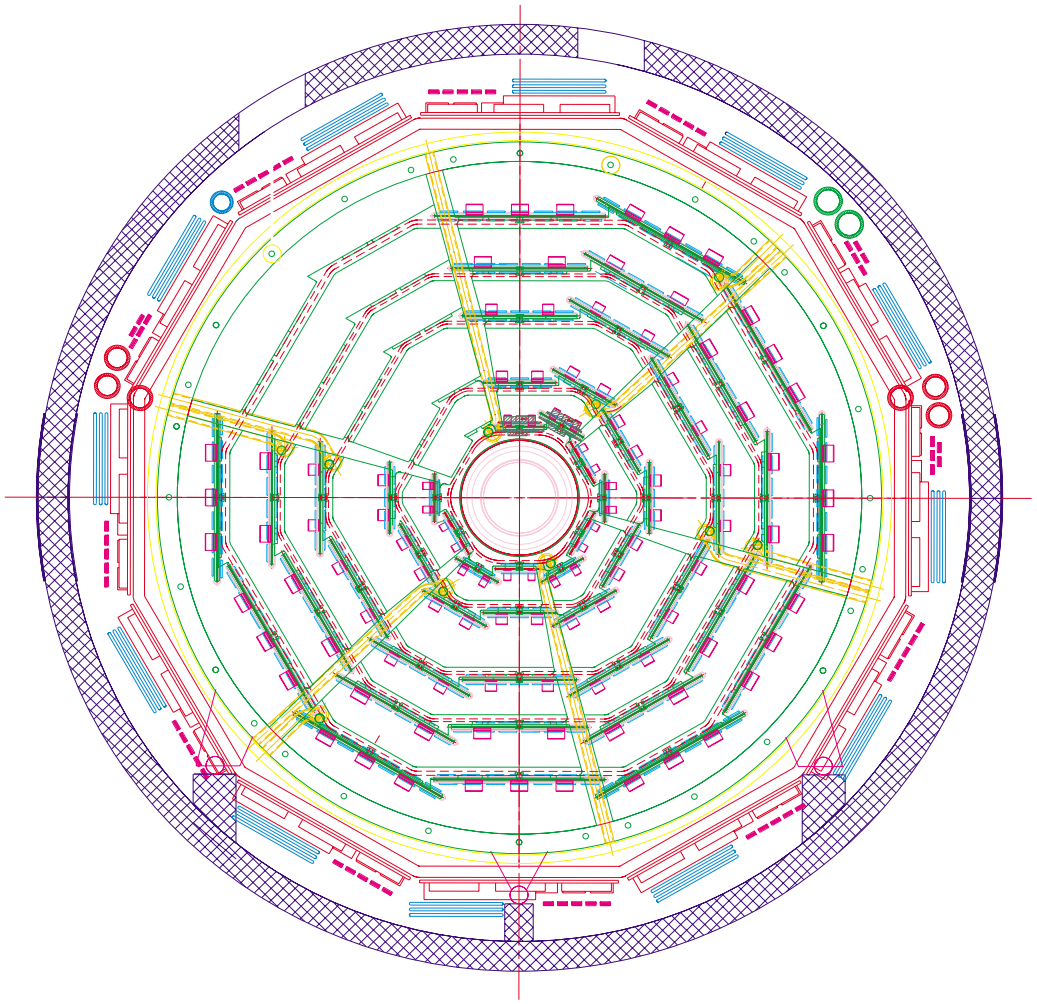


Quadrant of CDF Run 2a tracker

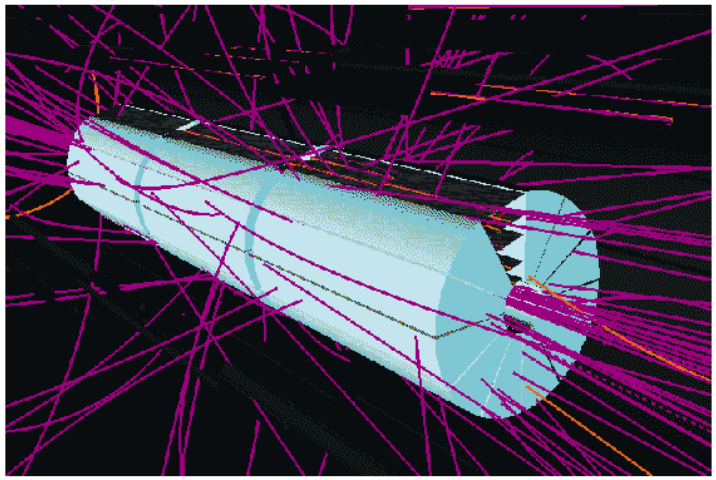
(Arrows point to silicon components)

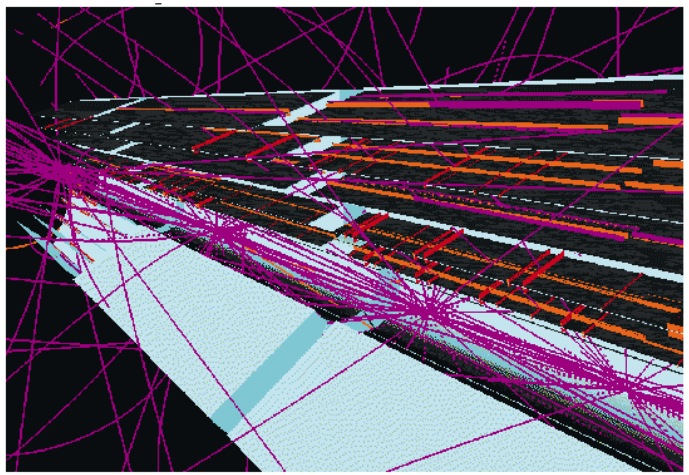
SVX II: 3 Barrels, 5 Layers

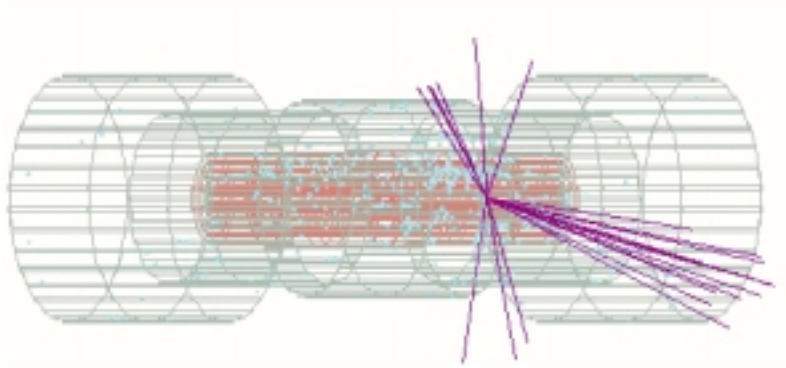


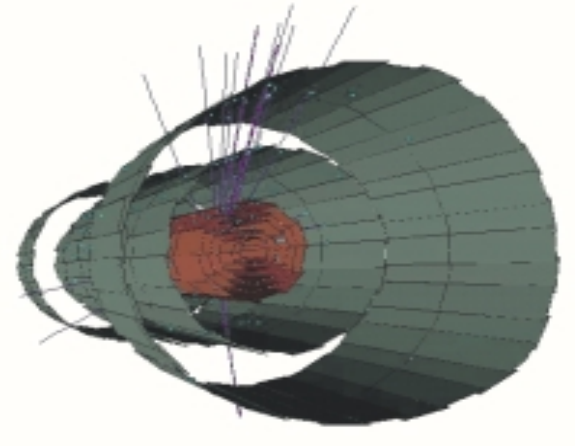


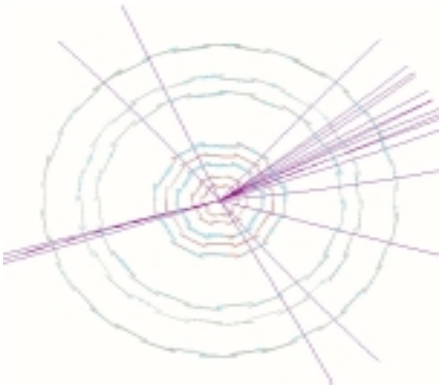
Simulation: Run II CDF Si









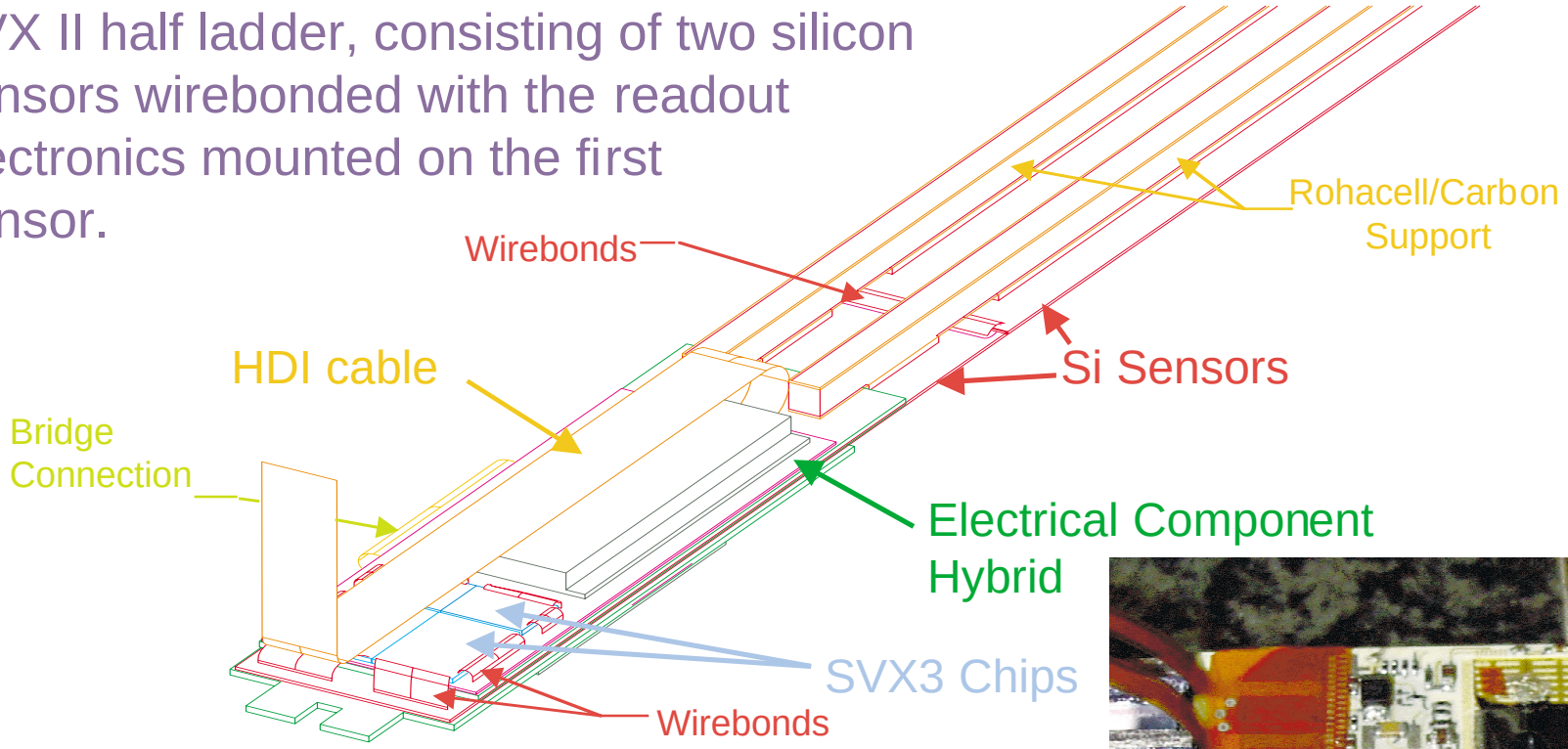


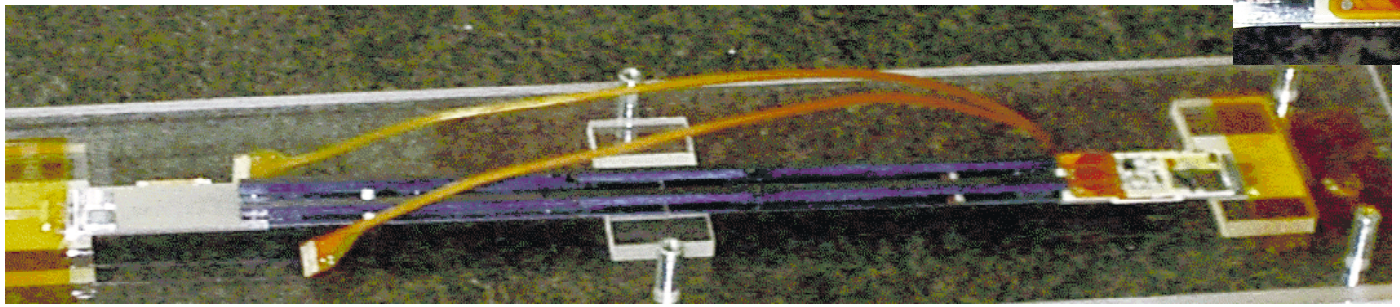
Open Inventor based

ROOT based

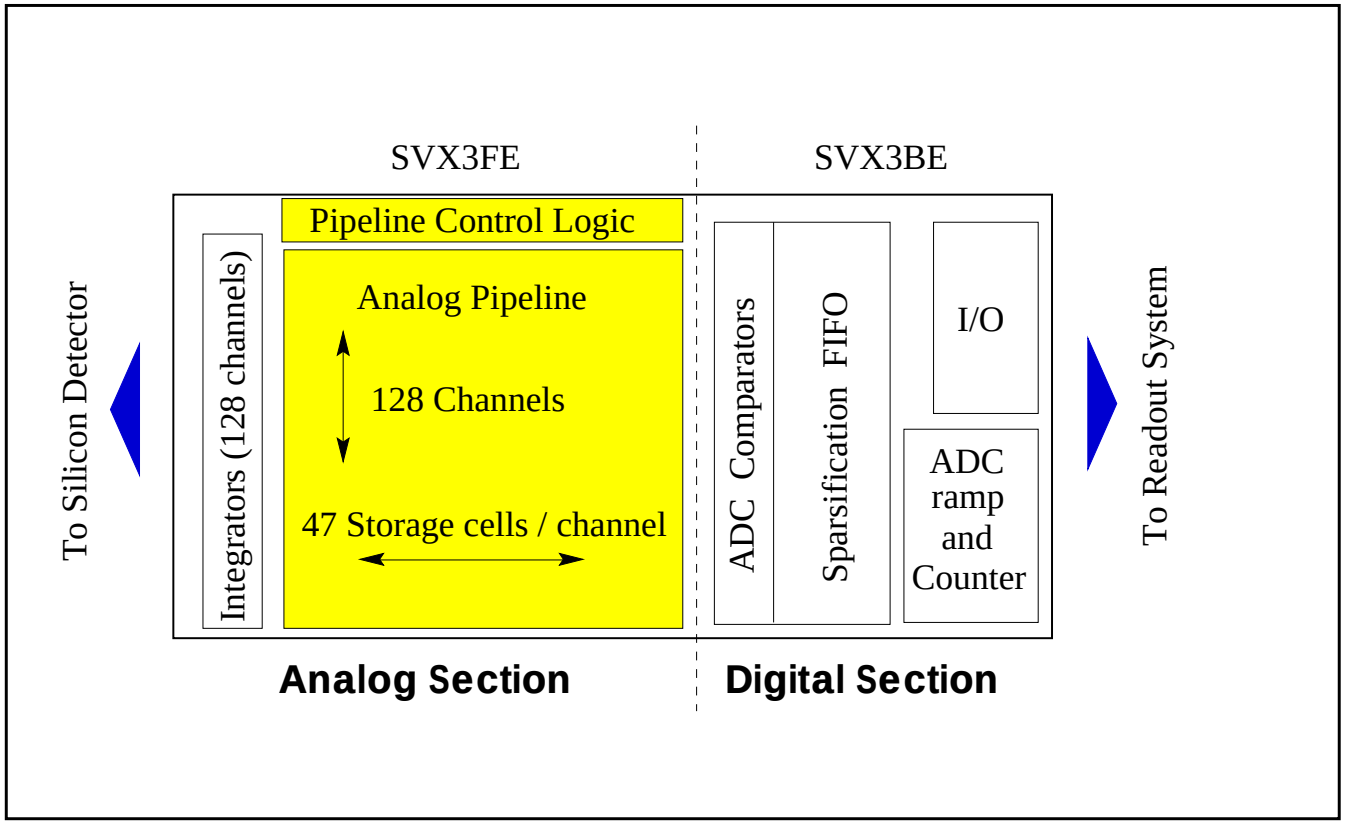
SVX II Ladders

SVX II half ladder, consisting of two silicon sensors wirebonded with the readout electronics mounted on the first sensor.



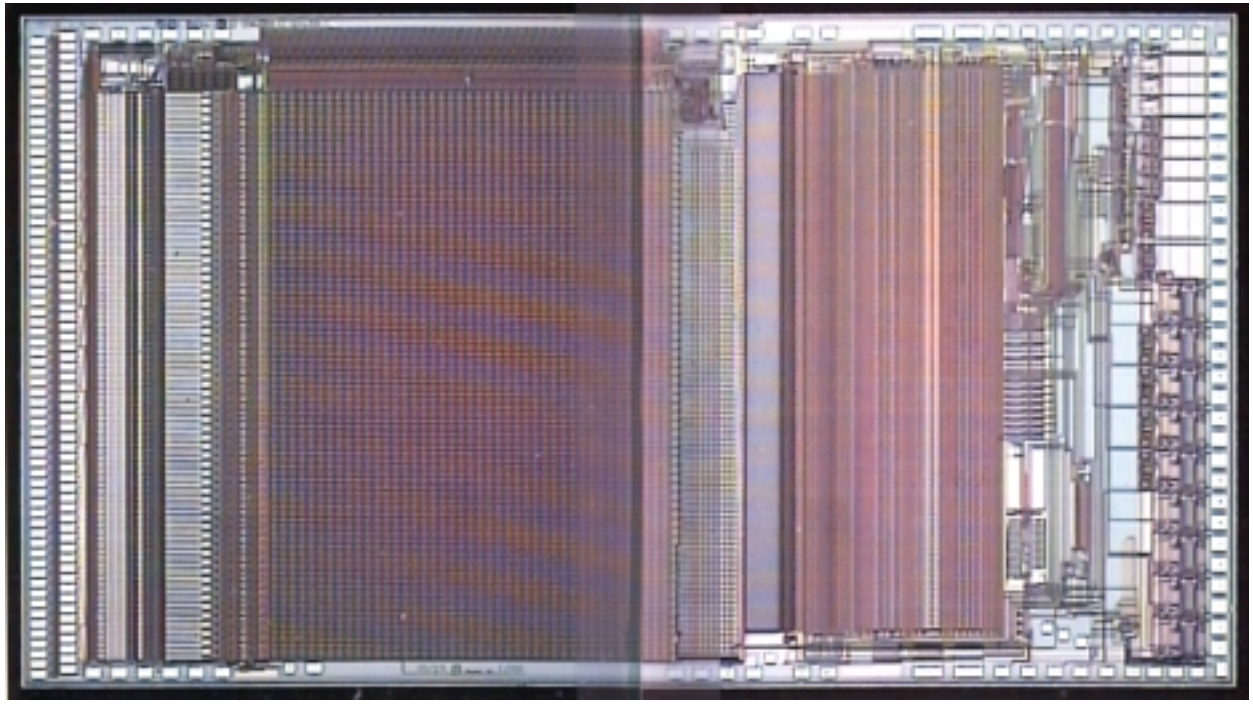


SVX3D R/O Chip



- Rad-hard 0.8 um Honeywell CMOS
- Tested to ~ 4 MRad
- Deadtimeless
- Dynamic pedestal subtraction
- Common to all Run II CDF silicon projects

SVX3D R/O Chip



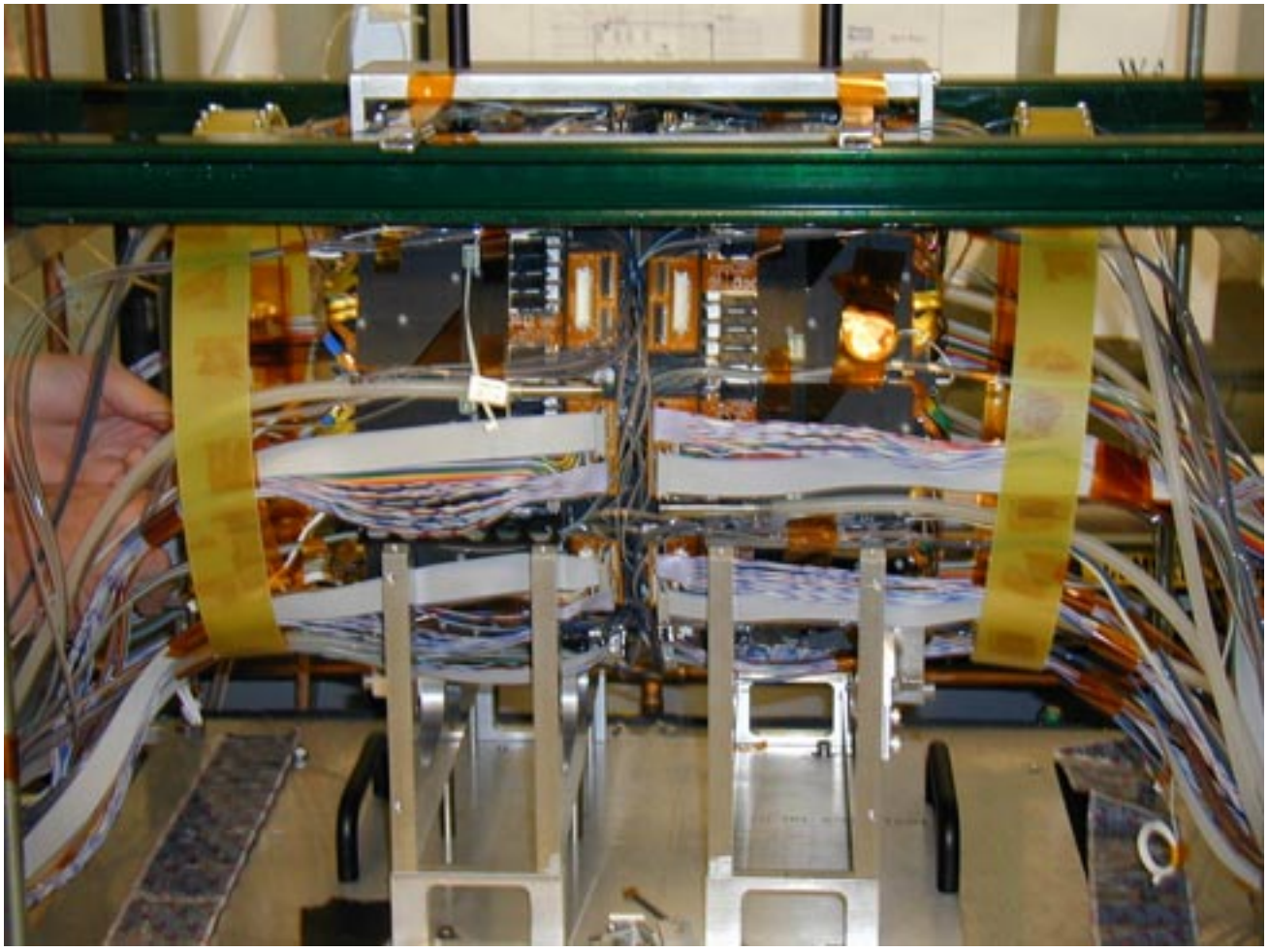
UCD Students on Run IIA Silicon

- UCD students on Run IIA silicon (ISL and Layer 00):
  - Sasha Barioant
  - Paul Gomez (UG, post-graduate researcher)
  - Chris Hill (graduated, now at UCSB, co-leader of CDF Silicon)
  - Tiffany Wilkes

Right:
Chris Hill at work on his thesis

Last Collab Meeting…

- SVX looked like this:



2 barrels in spacetube and working to finish Barrel-3

Last Collab Meeting…

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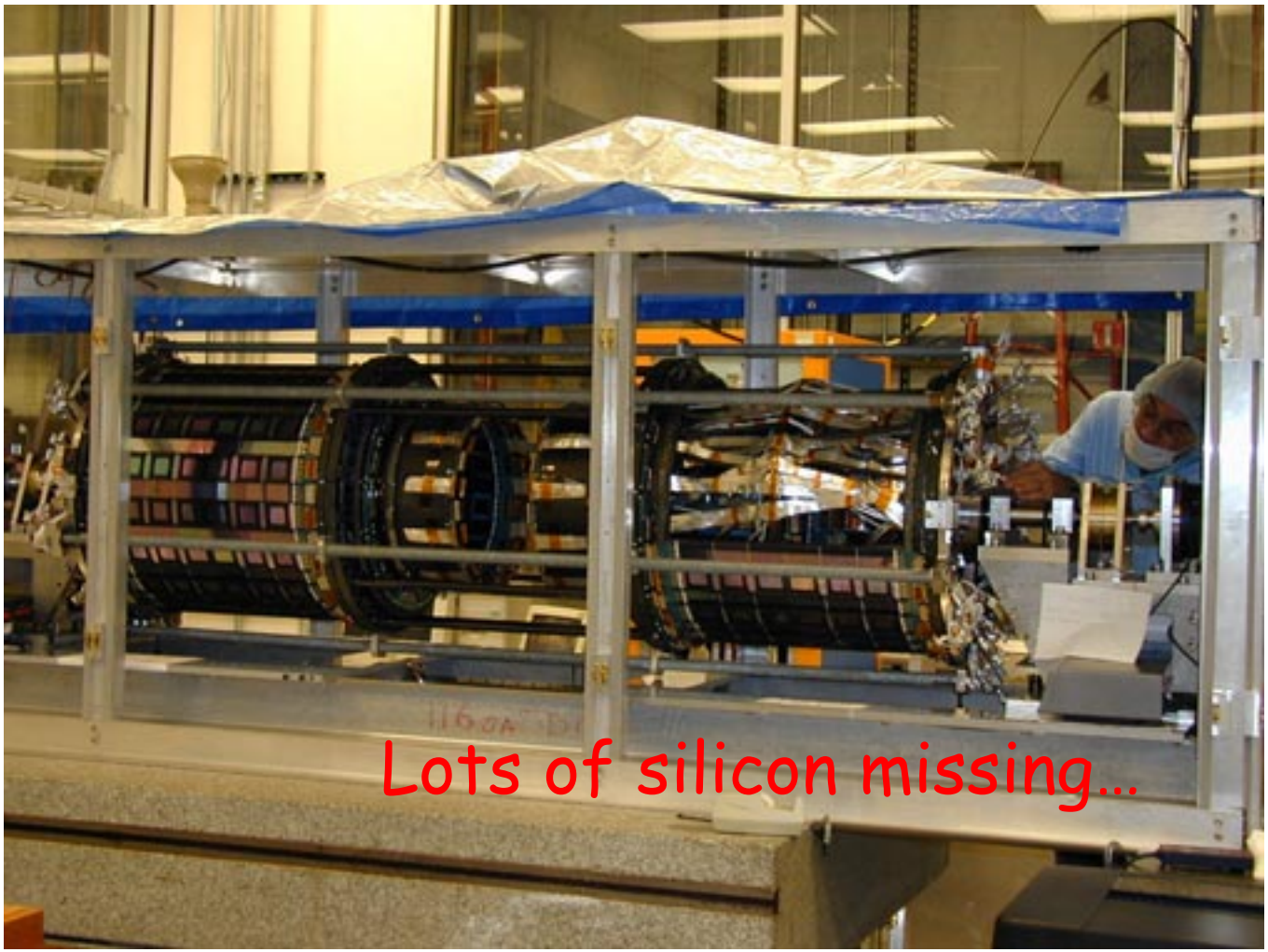
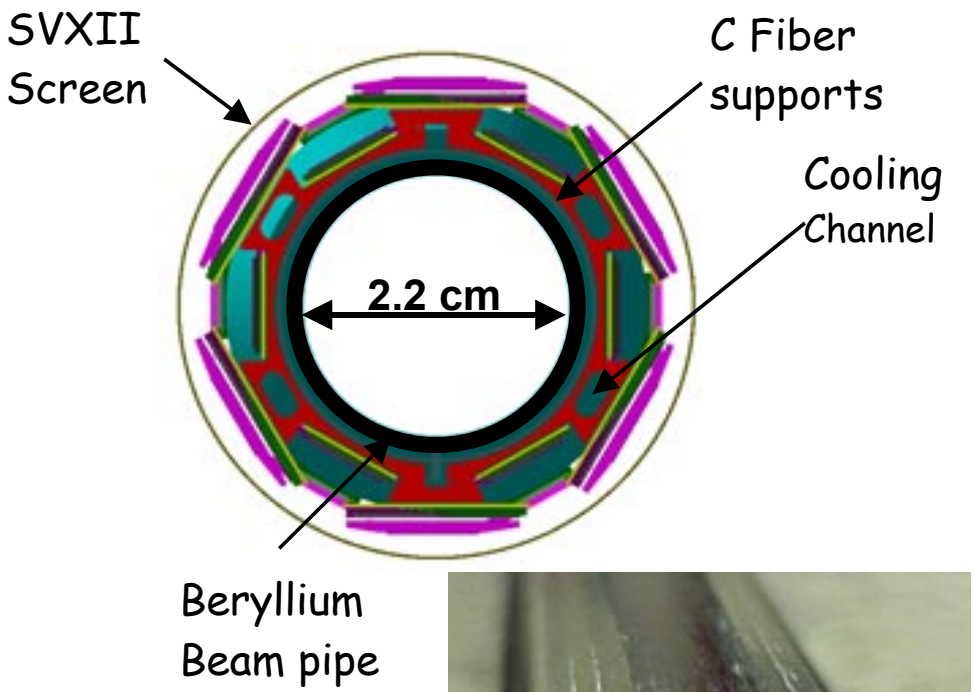


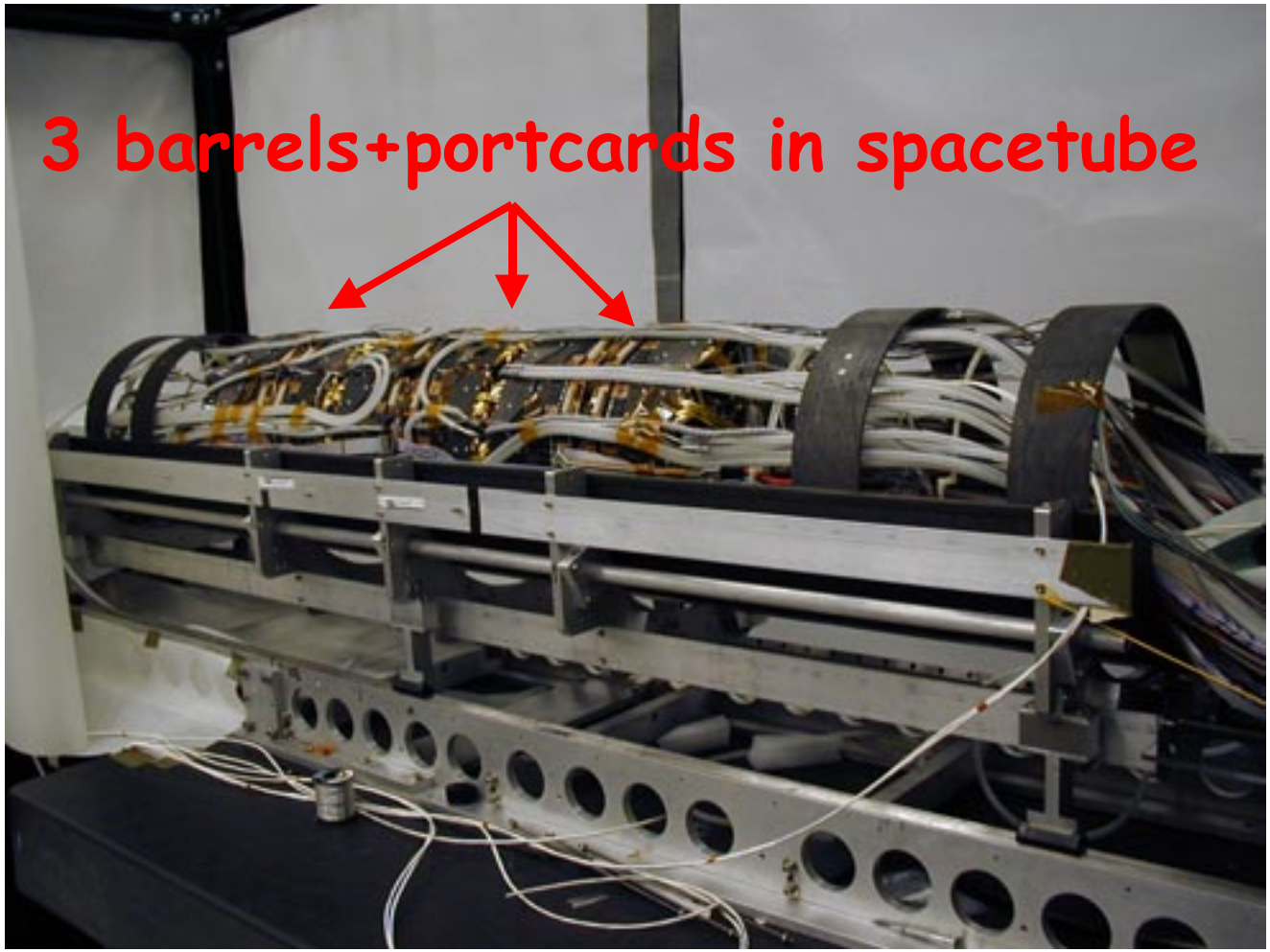
Last Collab Meeting…

- Layer 00 was still a cartoon…



About 2 wks later…

- SVX looked like this:



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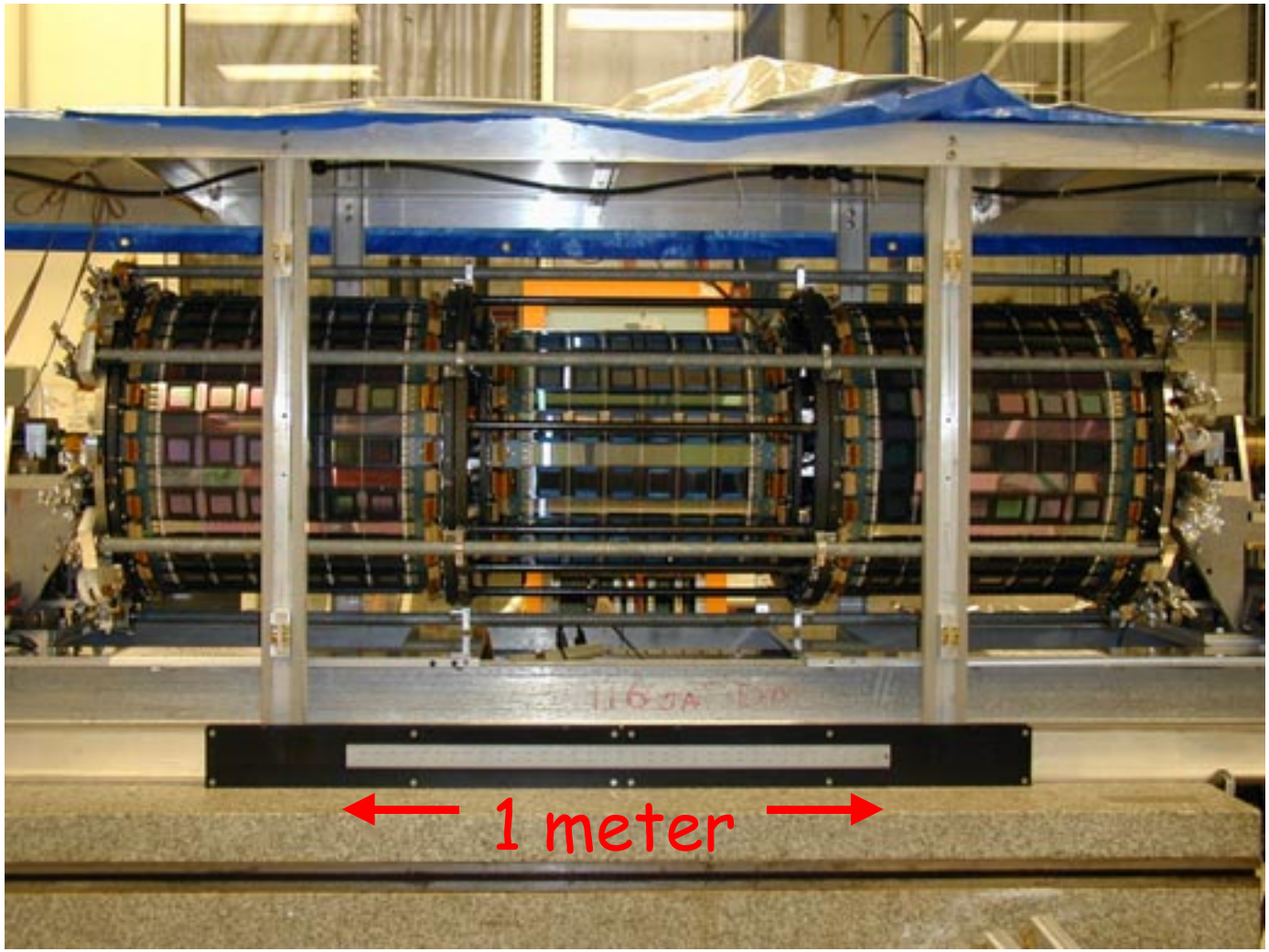
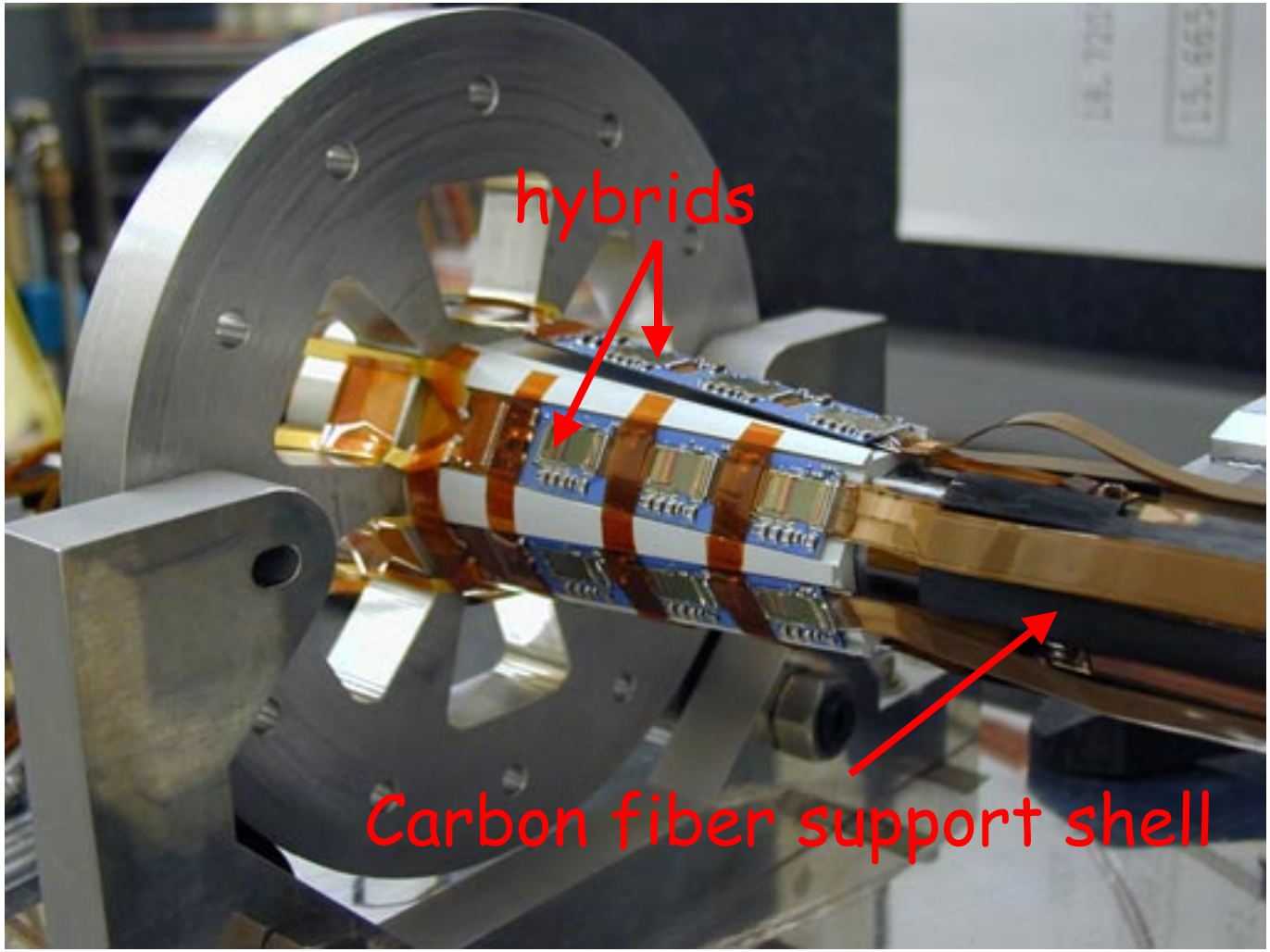


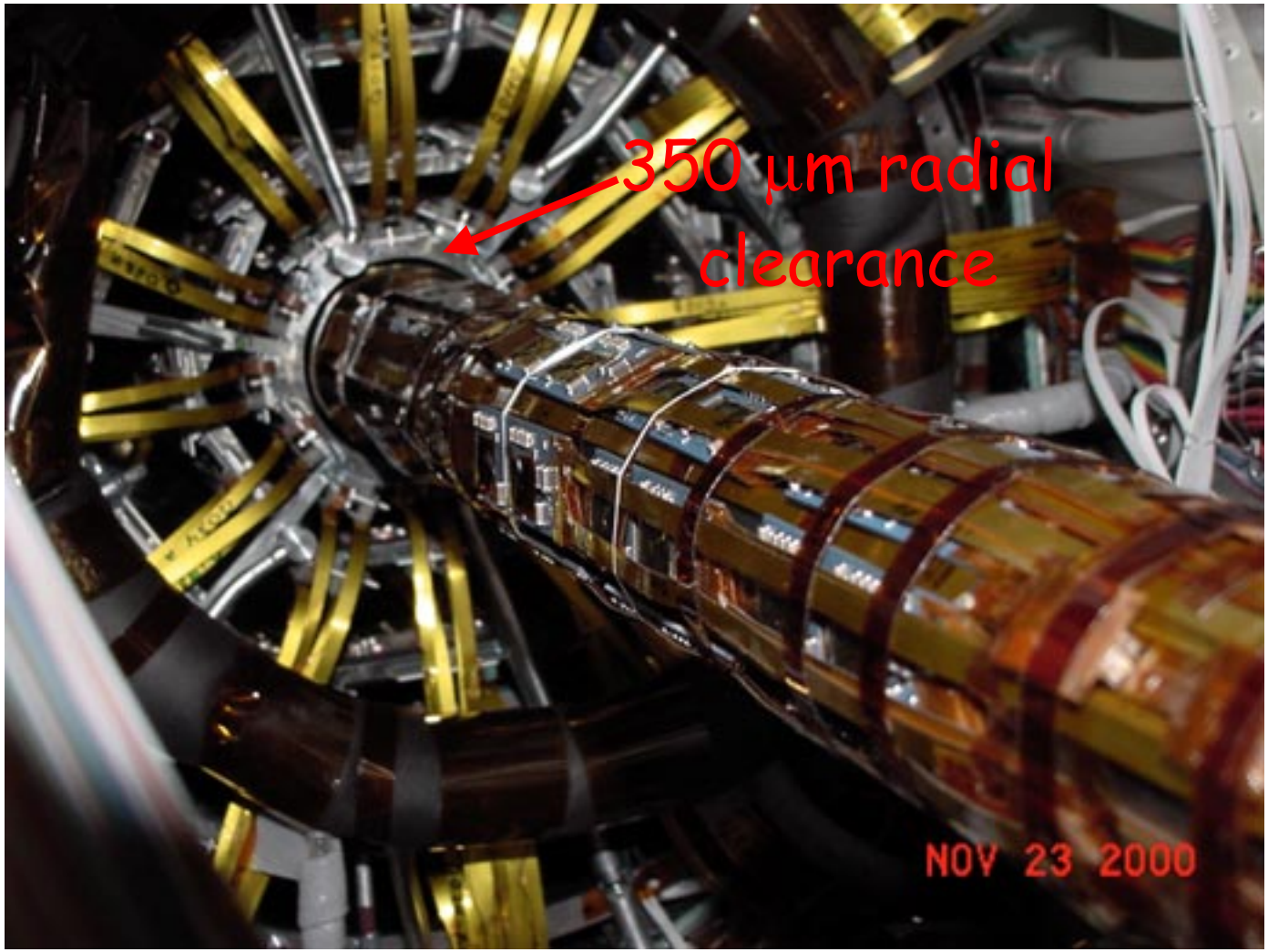
By November…

- L00 looked like this:



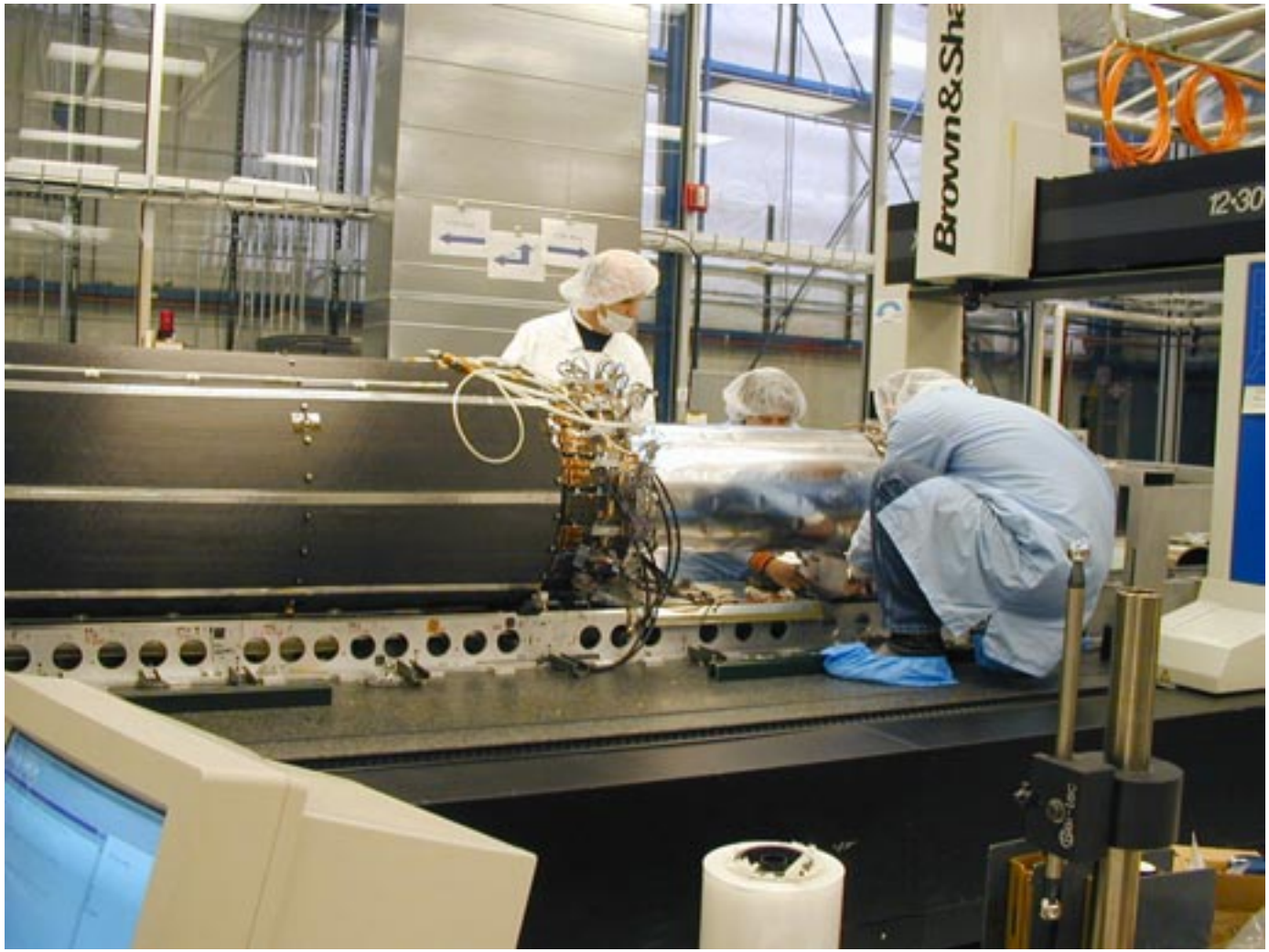
By end November…

- L00 installed inside SVX:



By end December…

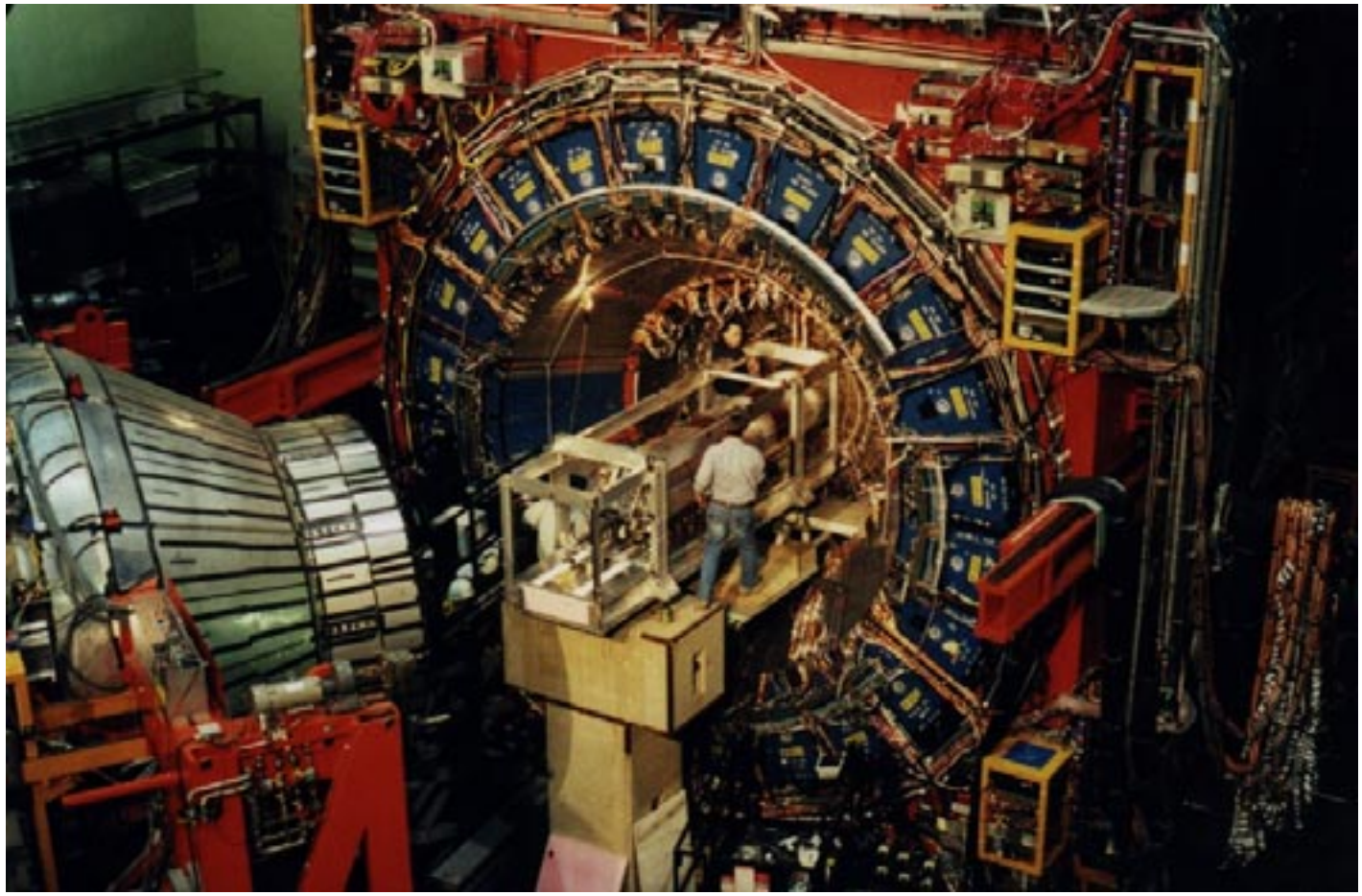
- SVX/L00 installed inside ISL:



16-January-01: The Move

everything went exactly as planned -

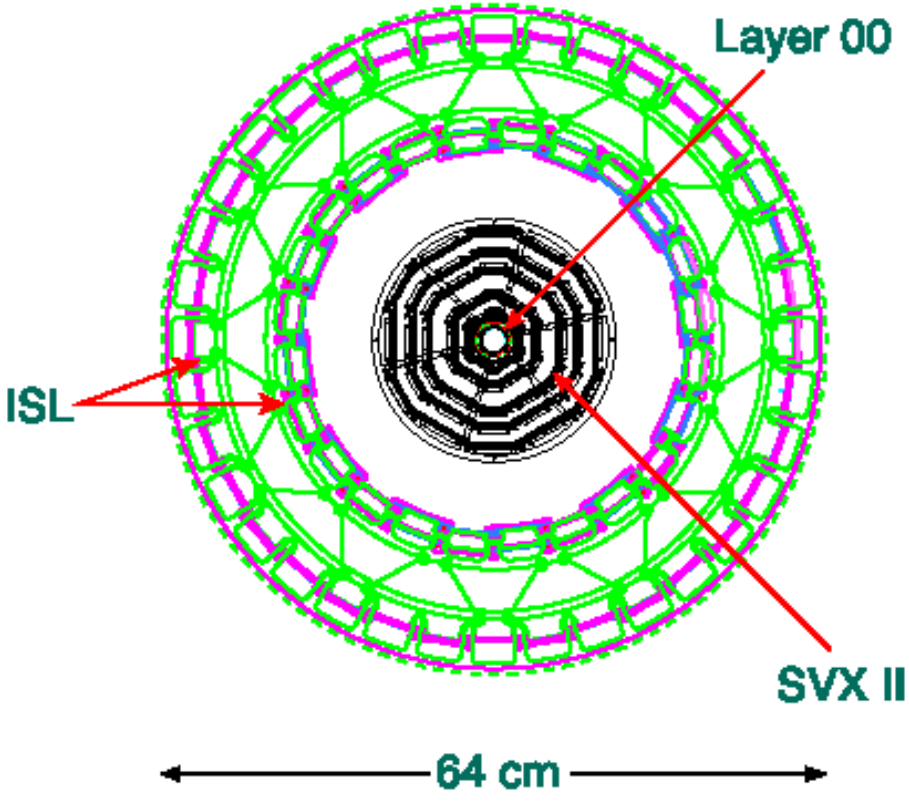
16-January-01: The Installation



The CDF Run2 Silicon Detector was installed inside the COT at around 2200 on 16-Jan-01

Current CDF SVX and Run 2b

- CDF now collecting data in Run 2a
- More luminosity needed for high mass searches
- Upgrade accelerator and aim for ≥ 15 fb^{-1}: **Run 2B**
- **CDF modifications needed to handle rate and radiation damage**
- UC Davis part of SVX upgrade group from inception
- Plan to install upgrades in 2005

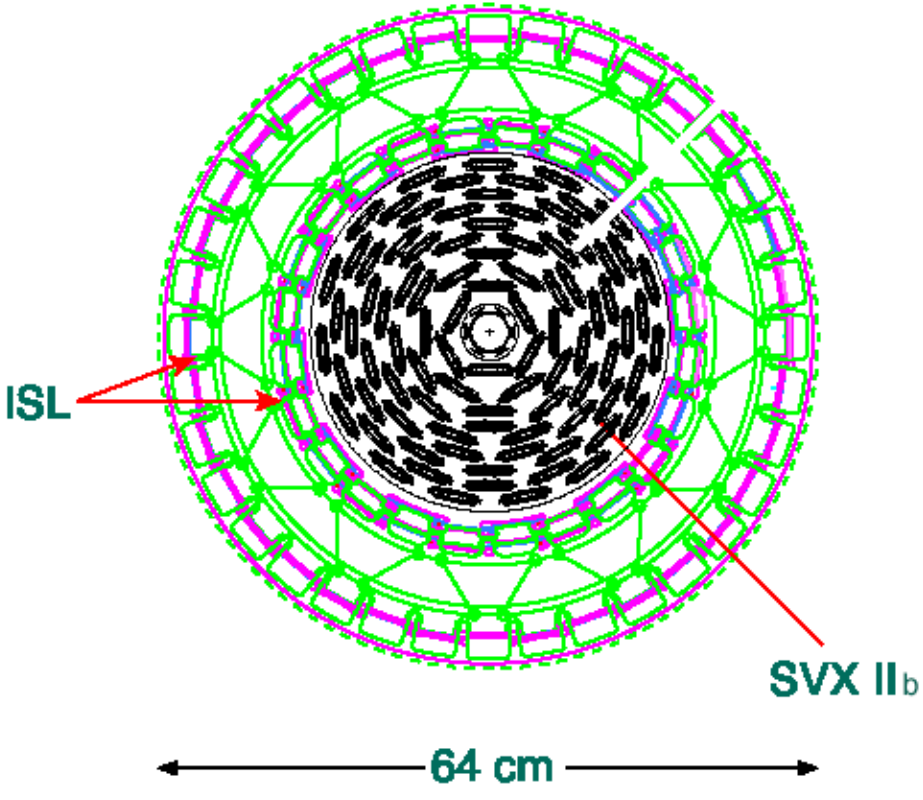


CDF Run 2a SVX inside ISL

(System designed for 2 fb^{-1})

CDF Run 2b SVX Upgrade

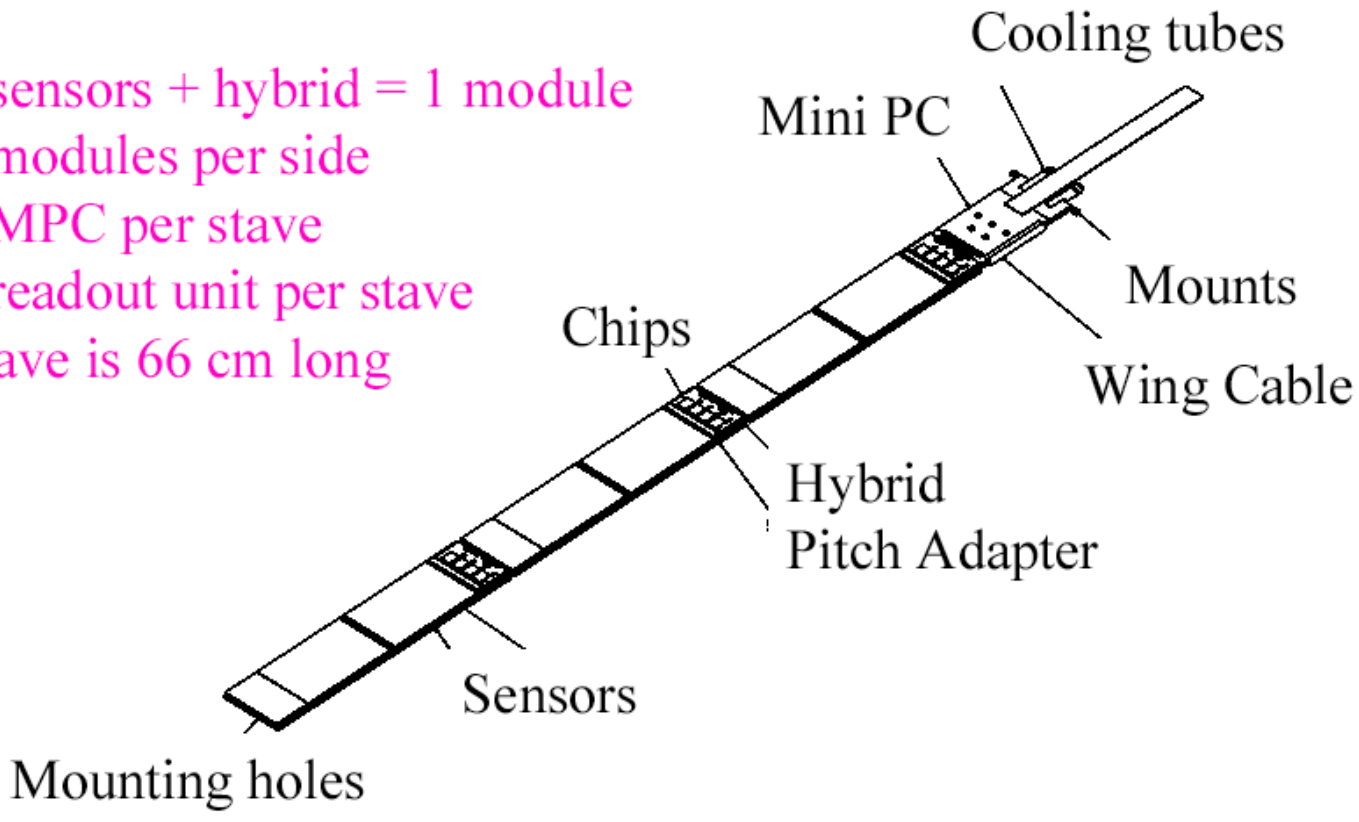
- Inner SVX2 layers will begin to fail after 4 fb^{-1}
  - Replace sensors with HV single-sided strips
  - New SVX4 readout chip in 0.25 μm technology
- Must replace SVX as a complete package
  - Minimize accelerator down time
  - Minimize risk of breakage
- Modular design with **staves**
  - Uniform staves simplify construction
  - Maximum use of space inside ISL



Proposed Run 2b SVX in ISL

Stave Design

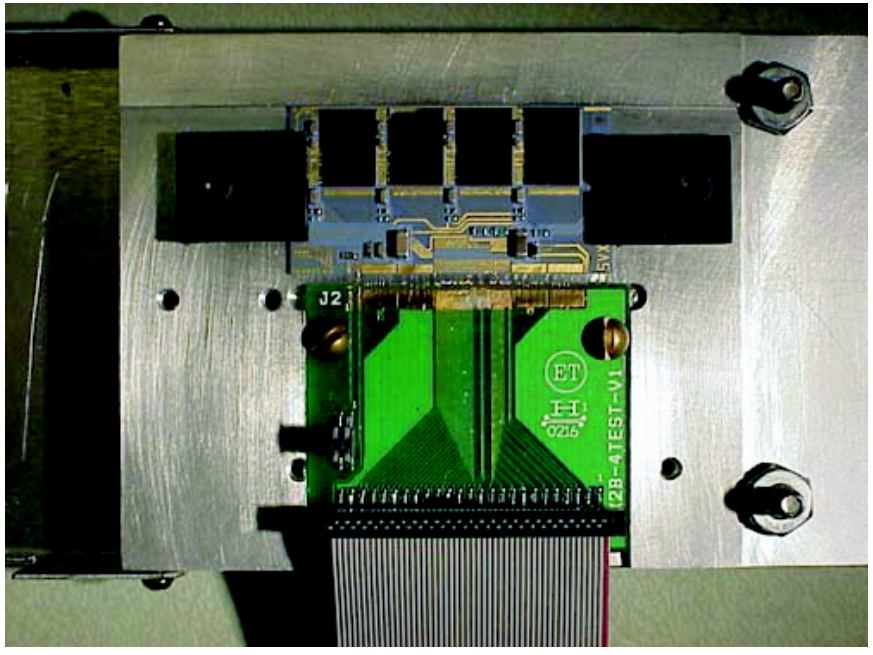
- 2 sensors + hybrid = 1 module
- 3 modules per side
- 1 MPC per stave
- 1 readout unit per stave
- Stave is 66 cm long



- Stave extends half the length of the barrel to central bulkhead
- All outer layers use this design (180 staves); inner layer on beam pipe
- UC Davis working with SVX4 readout chips and hybrids

Outer Layer Hybrid

- Run2b SVX has 1080 4-chip hybrids like this one for outer layers
  - Chips will be wire bonded to sensors along top edge
  - Hybrid will connect to bus cable running underneath on stave
  - Hybrid material is BeO with fine-pitch traces to interconnect components
  - Mounted in aluminum box for testing and burn-in
- Inner layer ("layer 0") has 72 similar 2-chip hybrids



4-Chip Hybrid in Test Module

(Green board is fanout for test connector)

SVX Stave Construction Plan and Schedule

- R&D and prototyping are under way on rapid schedule
- Plan two stave prototype rounds, preproduction before final production
- Each round requires all stave components including hybrids
- UC Davis Task: Hybrids must be operated and monitored for ~ 72 hours ("burn-in") prior to use in stave assembly. Failing hybrids must be debugged. Need 40 hybrids/week during production.

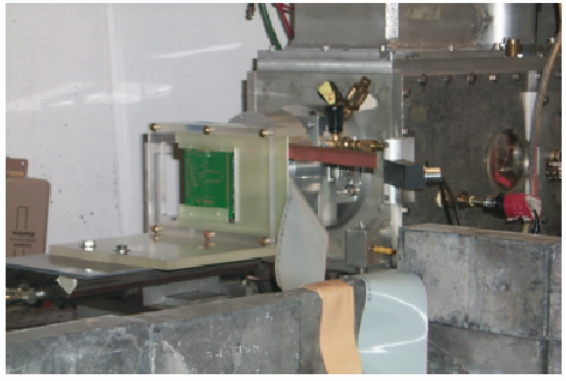
Run 2b SVX Project Critical Path Summary

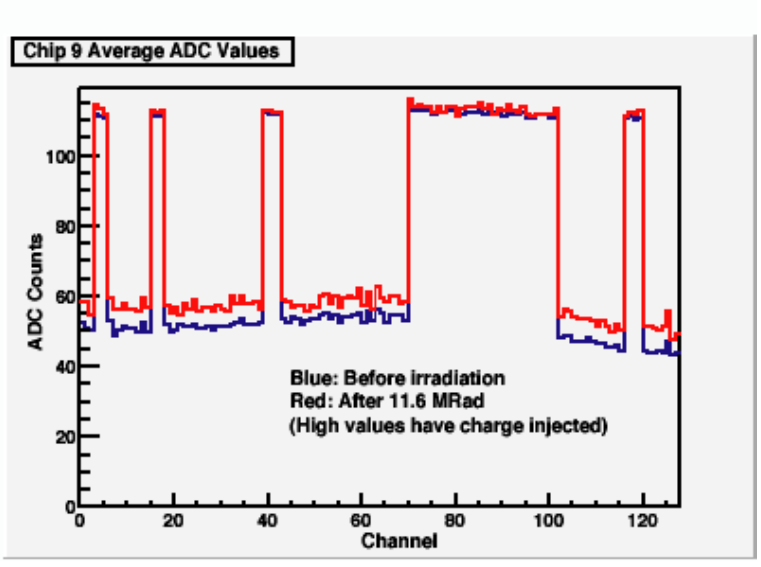
Task Name	Duration	Start	Finish
Stave Prototype Round 1	126 days	7/15/02	1/21/03
Stave Prototype Round 2	120 days	1/22/03	7/10/03
Stave Preproduction Round	131 days	7/11/03	1/28/04
Stave Production	245 days	1/29/04	1/21/05
Installation	135 days	8/23/04	3/11/05
Final Assembly	50 days	3/14/05	5/20/05

Assumes Run 2a ends 1/1/05, CDF ready to install SVX 3/14/05

SVX R&D at UC Davis

- Have set up Linux test stand for SVX4 chip and hybrid at UC Davis
  - Designed buffer for Linux computer
  - Wrote code for SEU and ^{60}Co tests
- Measured SEU cross section at UC Davis cyclotron (63 MeV protons)
  - Based on 4 SEU's observed, $\sigma_{SEU} = 6 \times 10^{-17}$ cm^2
  - Lower than for SVX3 in same beam
  - Conclude SEU-resistant chip design successful





Top: SVX4 chip in UC Davis cyclotron beam

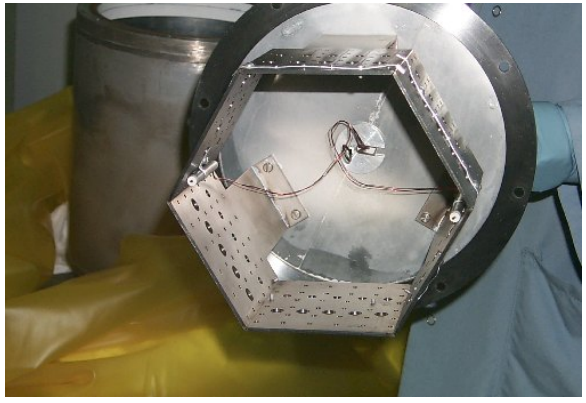
Bottom: Analog performance after 11.6 MRad

SVX R&D at UC Davis II

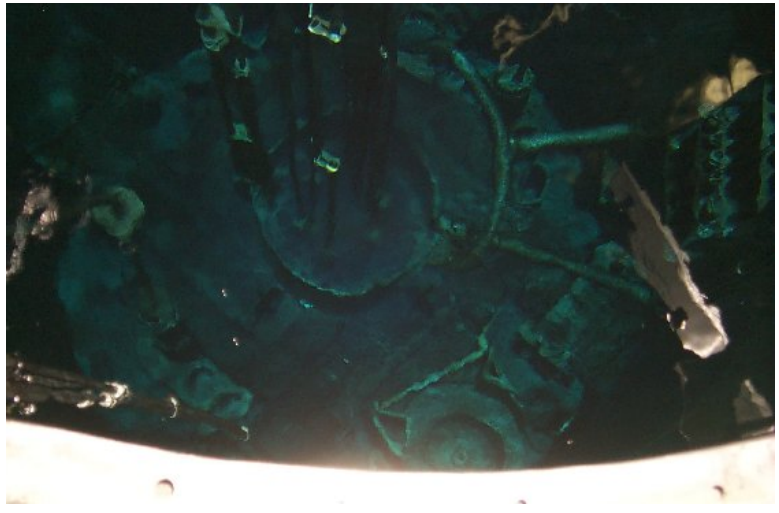
- With LBL, tested SVX4 chips and hybrids with ^{60}Co gammas, wrote code for analysis.

- Irradiated prototype sensors to 1.4×10^{14} n/cm^2 (1 MeV-equiv.) at UC Davis MNRC reactor

- Expect to continue irradiations of sensor samples for quality control during prototype and production rounds



Sample holder for 1 MeV neutron irradiation



Peering down into MNRC reactor core

UC Davis Major Task–Hybrid Burn-In: Logistics

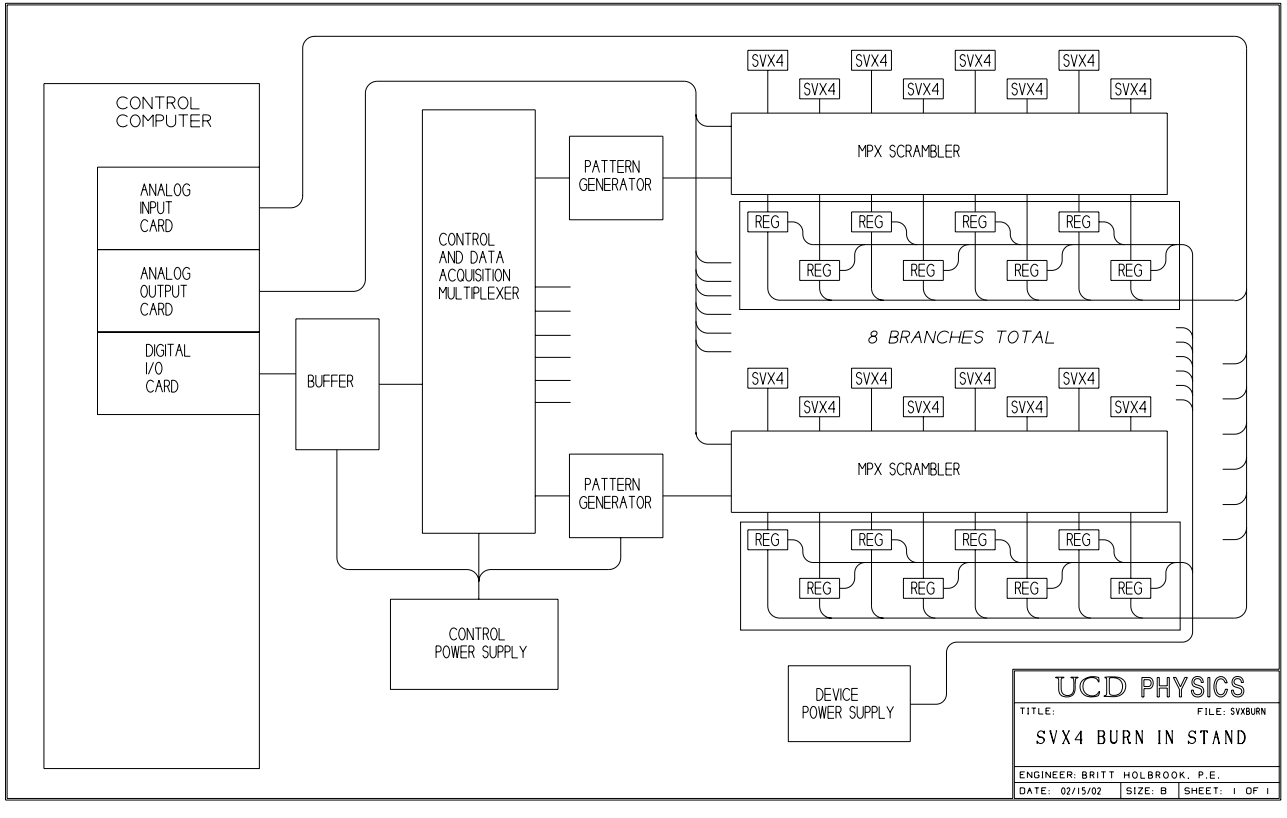
- Hybrids fabricated and checked at LBL, sent to UC Davis for burn-in
  - UC Davis will burn in all hybrids required for the upgrade
    - 1080 4-chip hybrids and 72 2-chip hybrids plus prototypes and spares
  - Burn-in includes performance monitoring and record keeping
  - Monitor supply current, turn off modules which fail
  - UC Davis will diagnose hybrids whch fail, return them to LBL for repair
    - *e.g.*, chip or other component replacement, wire bond repair,. . .
- Hybrids passing tests sent to Fermilab for module and stave assembly

Burn-In Hardware Requirements

- For Run 2a, burn-in done at LBL
  - 40-port burn-in stand connected to SGI computer by CAMAC interface
- Will build on this but need modifications and new hardware due to:
  - 2.5 V power supply for SVX4 (instead of 5 V)
  - Connections are different for the SVX4 hybrids
  - Move to Linux/PCI rather than SGI/CAMAC
- Requires
  - New buffer and interfaces to computer
  - New multiplexed hybrid interconnection boards ("MPX scrambler")
  - New power supply regulator/monitor boards
  - Modified control program (!)
  - Mechanical support and cooling (via fans)

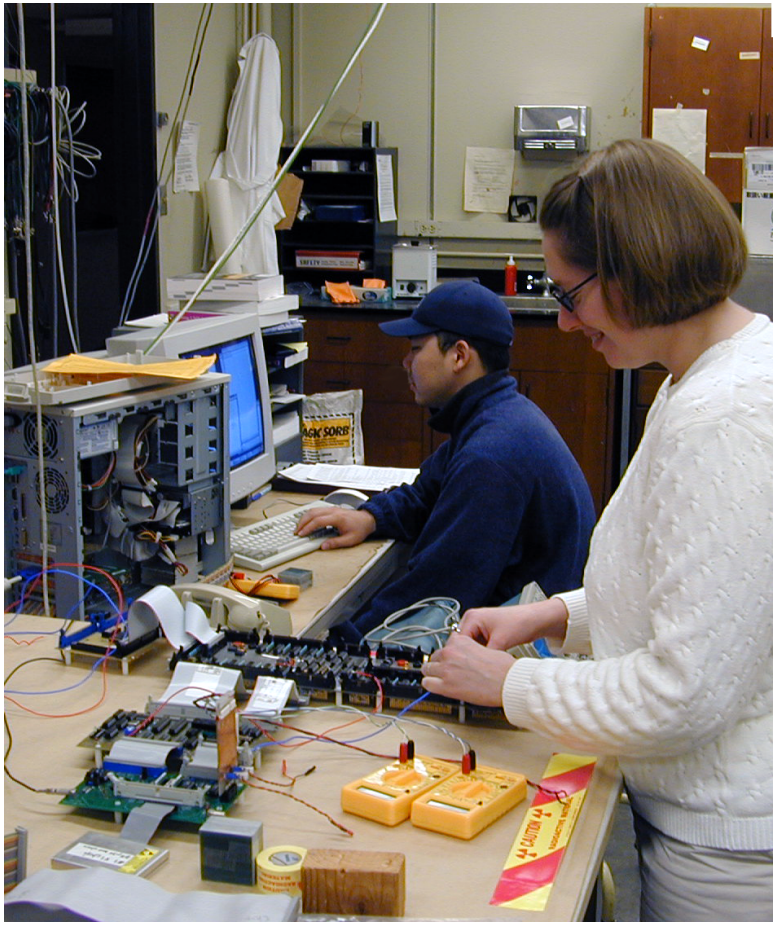
New Burn-In Stand Block Diagram

- Major components: computer, buffer, control and DAQ multiplexer, pattern generator boards, MPX scrambler boards, regulator cards (red means new)



Current Tasks

- Design and lay out new burn-in stand
- Assemble prototype stand based on former LBL system
  - Use as test bed for burn-in software conversion
- Modify hybrid testing software for use with single test stand
- Fabricate burn-in stand
- Prepare to begin operations for preproduction rounds



Tiffany Wilkes and Wajohn Yao prepare to test control and DAQ MPX

UC Davis Schedule and Milestones

- Milestones for burn-in stand
  - January 2003 – Burn-in stand design complete
  - April 2003 – Burn-in stand complete
- Tasks in 2003
  - Complete burn-in stand
  - Includes software development
  - Pre-production practice
- Task in 2004: Production

–UC Davis making key contributions to CDF Run 2b upgrade