Hybrid preproduction/testing

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Brief Overview

more detailed status report tomorrow, now concentrate on:

- **workflow**
- common **hardware** and **test procedures**
- **schedule**

Workflow

- wafer production at TSMC
- **wafer probing** at **FNAL**, dicing + delivery to CDF (LBNL) and D0
- preproduction of 180 (bare) BeO hybrids by CPT
  - delivery of 116 promised for this week
  - only minor/ cosmetic changes wrt 1. version
- **stuffing** with SMDs and SVX4 die attach
  - 2 options: AA and LBNL engineering division (try both)
  - after this step: visual inspection and check for opens/shorts on power traces
- **bonding** of stuffed hybrids
  - 3 options: Amtech, Promex, LBNL engineering division (try all in parallel for the start)

- hybrid **performance tests** at **LBNL**
  - visual inspection, check for opens/shorts on power traces: ~ 2 min/ hybrid
  - fast check of pedestal/ charge injection/ noise levels, and readout errors: ~ 5 min/ hybrid
  - extensive automized testing using htest
  - ~20 min/hybrid, 2 hybrids in parallel => **< 2 hours/day** at nominal rate (**40 hybrids/week**)
- **burn in** at **UC Davis** -> Davis talks
  - **~ 72 h of burn in** (= power+ continuous run of pattern)
  - can soon run 2x8 hybrids in parallel => rate: **~ 32 hybrids/week** (assumes 6 days/week, 72 h)
  - eventually 8x8 hybrids in parallel
- **final test** at **FNAL**
  - use **PTS** (proof consistency with CDF DAQ eventually)

Common hardware and test procedures

=> use **same tools** (code, hardware, procedures, data base) as much as possible

=> need **good communication**

- **test code:** everyone is using htest package
  - was some effort but will be very beneficial

- **selection of tests:** try to run consistent/identical subsets of tests where possible
  - not everyone makes power consumption tests
  - wafer probing is a bit different due to more challenging electrical environment and time constraints

- **hardware:** as similar as possible
  - same frequency is desirable (40 or 50 MHz)
  - very similar DAQ systems at FNAL (wafers), UC Davis, LBNL
  - PTS is quite different, so have a cross check!

- **database** -> Wajohn's talk
  - joint UC Davis/ LBNL project
  - important role in preprod.
  - currently data base contains info on:
    - wafer probing
    - hybrid assembly, test and burn-in,
    - bus cable …

Initial Schedule (it's hard to predict the future)

- have enough **chips** for now, will get more soon
- CPT will deliver **hybrids** this week **~ July 30**
  - will deliver inspected hybrids to AA/ LBNL engineering within days
- need to use **database** within a week !
  - want to use db from the very start, will have paper backup
- get **stuffed hybrids** **~ Aug 12**
  - need a few days at LBNL for inspection and db
- delivery sets of 5-10 hybrids to 3 bonding sites
- get **bonded hybrids** back **~Aug 25**
  - ~1 week of testing at LBNL before first delivery to UC Davis
- **burn-in done** **~ Aug 30**
- OK from test at **FNAL** **~ Sept 5**

- **biggest uncertainty is fraction of repairs …**

- Emphasize **quality** over speed

(working in parallel should increase effective rate)

- decide on 'Who get's which share' only after first test round **~ by Aug 30**
- feed to **finish db** and start using it ~ 7 days
- need to **streamline test procedures** ~ 14 days
- Get **PTS** to run htest ~3 week
  - looks good -> Tom's report

- other activities: Co-60 and SEU tests, bus cable, chip testing

Are likely to have our hands full for a while !