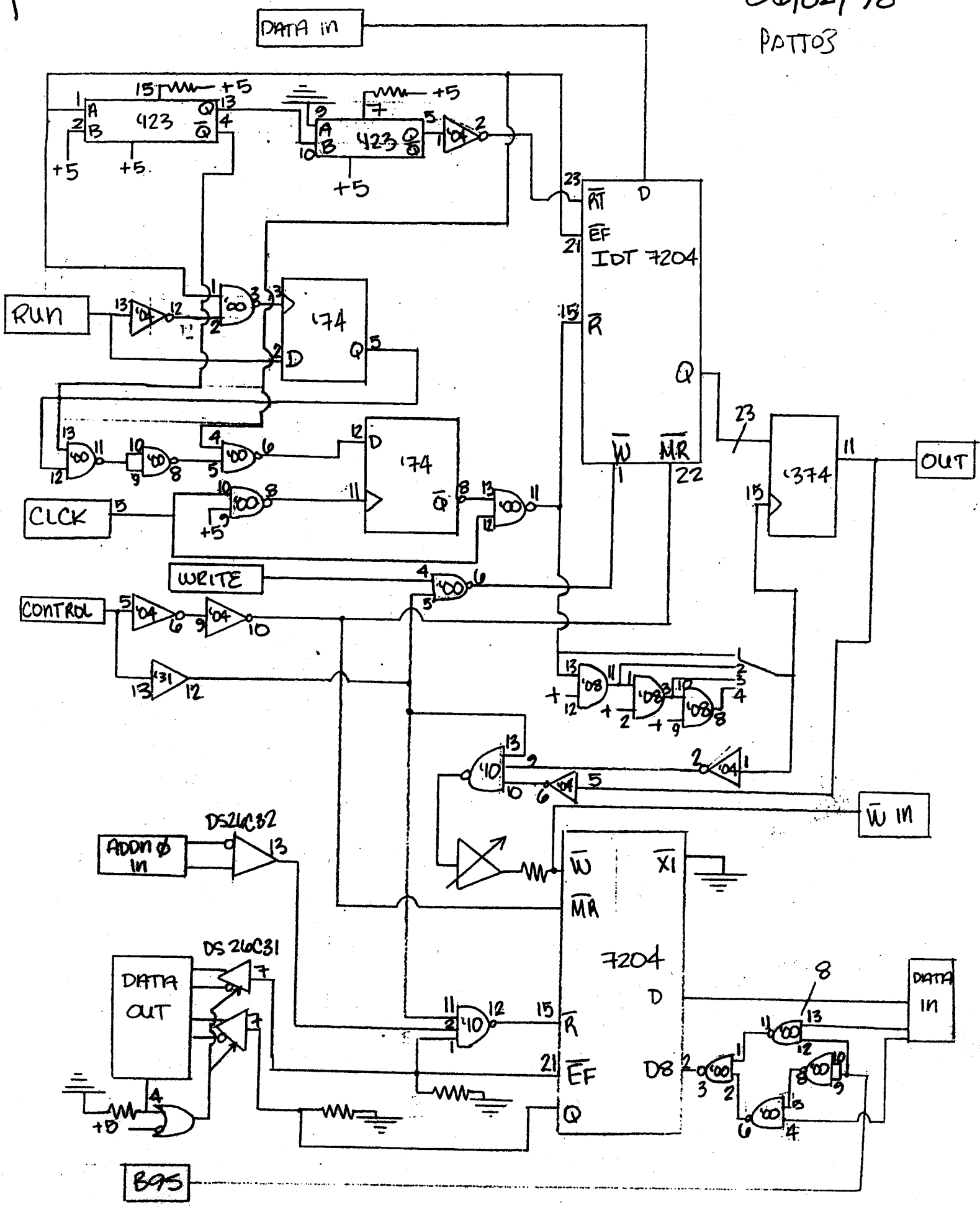


PATT BOARD

06/02/98

PATT03



PAT02 board connector pinouts

NOTE THIS

IC PAT02

AND NEEDS

VERIFICATION

60-pin connector input

Even number pins are ground

Odd number pin signals:

- \*1 control
- \*3 run
- 5 write
- \*7 retransmit
- \*9 bit 9 select
- 11 data 0
- 13 data 1
- 15 data 2
- 17 data 3
- 19 data 4
- 21 data 5
- 23 data 6
- 25 data 7
- 27 data 8
- 29 data 9
- 31 data 10
- 33 data 11
- 35 data 12
- 37 data 13
- 39 data 14
- 41 data 15
- 43 data 16
- 45 data 17
- 47 data 18
- 49 data 19
- 51 data 20
- 53 data 21
- 55 data 22
- 57 data 23
- 59 n/c

Signals with a \* (eg. \*1) are asynchronous, while all others should be synchronous. For example, if using a Jorway 40 output register, use the 24 outputs of one channel to supply the "write" and data 0 through data 22 signals, and use any outputs from the other channel to supply "control" "run", "retransmit" and "bit 9 select".

34 pin connector output (next to 60 pin connector)

- |                       |                           |
|-----------------------|---------------------------|
| 1 n/c                 | 2 n/c                     |
| 3 clock input         | 4 clock input bar         |
| 5 empty fifo flag out | 6 empty fifo flag out bar |
| 7 bit 9 output        | 8 bit 9 output bar        |
| 9 bit 8 output        | 10 bit 8 output bar       |
| 11 bit 7 output       | 12 bit 7 output bar       |
| 13 bit 6 output       | 14 bit 6 output bar       |
| 15 bit 5 output       | 16 bit 5 output bar       |
| 17 bit 4 output       | 18 bit 4 output bar       |
| 19 bit 3 output       | 20 bit 3 output bar       |
| 21 bit 2 output       | 22 bit 2 output bar       |
| 23 bit 1 output       | 24 bit 1 output bar       |
| 25 n/c                | 26 n/c                    |
| 27 n/c                | 28 n/c                    |
| 29 n/c                | 30 n/c                    |

## 50-pin connector output

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Even number pins are ground

Odd number pins:

49	tristate (input)
47	raw clock output
45	data 0 output
43	data 1 output
41	data 2 output
39	data 3 output
37	data 4 output
35	data 5 output
33	data 6 output
31	data 7 output
29	data 8 output
27	data 9 output
25	data 10 output
23	data 11 output
21	data 12 output
19	data 13 output
17	data 14 output
15	data 15 output
13	data 16 output
11	data 17 output
9	data 18 output
7	data 19 output
5	data 21 output
3	data 22 output
1	+5V output

Note that there is no data 20 output, This signal is used internally for the "store" function that clocks data into the DAQ fifo. The "tristate" input has no effect if left floating. When pulled high it tristates the data 0 through 7 outputs.

## 34 pin connector input (next to 50-pin connector)

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1	n/c	2	n/c
3	n/c	4	n/c
5	n/c	6	n/c
7	n/c	8	n/c
9	n/c	10	n/c
11	input bit 1	12	ground
13	input bit 2	14	ground
15	input bit 3	16	ground
17	input bit 4	18	ground
19	input bit 5	20	ground
21	input bit 6	22	ground
23	input bit 7	24	ground
25	input bit 8	26	ground
27	ext. clock input	28	ground
29	bit 9 A	30	bit 9 B
31	n/c	32	n/c
33	+5V output	34	ground